System Block Diagram of GM7

POWER

REGULATOR +1.5V_SUS/+0.75V_DDR_VTT PG 30	CPU VCORE PG 29
+1.05V_RUN PG 32	DC/DC +3.3V_ALW/+5V_ALW/ +15V_ALW PG 33
+1.1V_RUN_VTT PG31	
SYSTEM RESET CIRCUIT PG 27	AC/BATT CONNECTOR PG 37
BATT CHARGER PG 28	GFX UMA PG 34
RUN POWER SW +3.3V_SUS/+5V_SUS +5V/+3.3V/+1.8V PG 36	+1.8V_RUN PG 35

FAN & THERMAL SMSC1422 PG 26

CLOCK SLG8SP585VTR (QFN-32) PG 02

USER INTERFACE PG 37

DDR3-SODIMM_A0 PG 13 — 1067/1333 MHz DDR III

DDR3-SODIMM_B0 PG 14 — 1067/1333 MHz DDR III

CPU/NB (Arranndale)

2 Core

(989 PGA)

PG 3-6

FDI(ARD) DMI X 4

PCH

(HM57)

PG 7,8,9,10,11,12

LVDS conn. PG 16

LVDS

HDMI Level Shifter SN75DP139RGZR PG 18

HDMI

DP

DB1 Conn.

PG 21

DP — DP Redriver SN75DP120 — DP conn.

HDMI — HDMI Redriver TMDS141 — HDMI conn.

PCIE[6] — LAN RTL8111EL — RJ45 conn.

SATA[4] / USB[1] — eSATA Redriver SN75LVCP412 — E-SATA Combo with USB CONN

PCIE[1] / USB[4] — MINI-CARD WLAN

PCIE[3] / USB[5] — MINI-CARD WWAN

Azalia I/F — AUDIO Codec ALC665 — Main SPK Amp MAX9736AETJ+ — Main SPK 1.5W*2

Subwoofer Amp MAX9736AETJ+ — SPK 3W*1

Audio Jacks X3 PG 39

E-Module Bay SATA - ODD PG 23 — SATA[1]

SATA - HDD0 PG 23 — SATA[0]

SATA - HDD1 PG 23 — SATA[5]

Bluetooth BTB Conn PG 32 — USB[8]

Card Reader conn. PG 17 — JMicron JMB389 PG 17 — PCIE[5] / USB[1,2,3]

PCIE[7]

USB conn. X3 — USB[1,2,3] — DB2 Conn. PG 22

USB 3.0 uPD720200F1

LPC

KBC ITE8502 PG 20 — 19X8 — Keyboard PG 24

SPI — FLASH 1Mbyts PG 30

PS/2 — Touchpad PG 24

SPI — SPI ROM 8M bytes PG 19

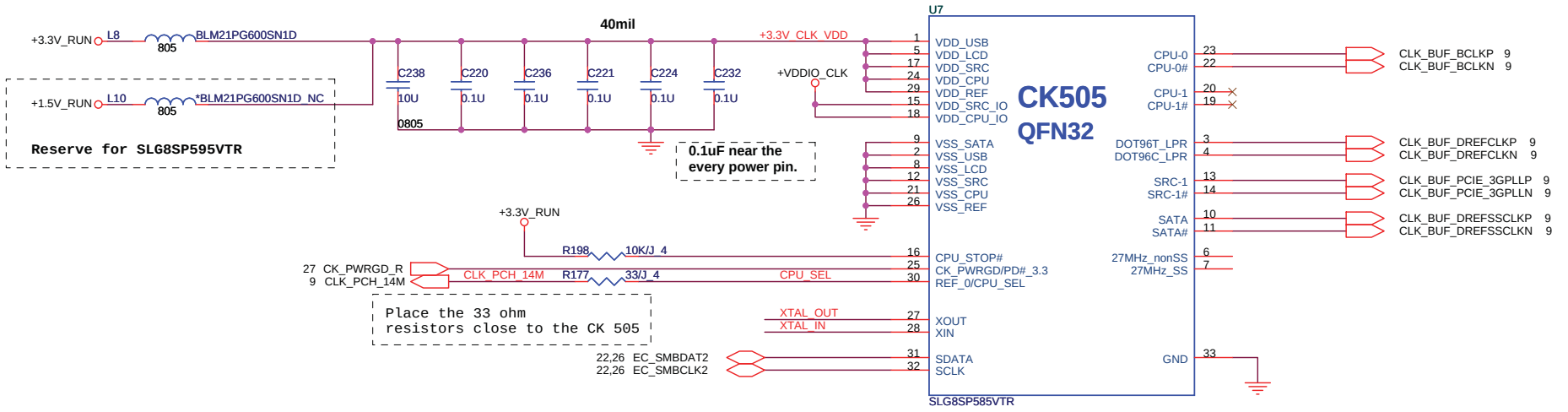
SATA[4] / USB[0] / PCIE[1,3] / USB[4,5]

Azalia I/F

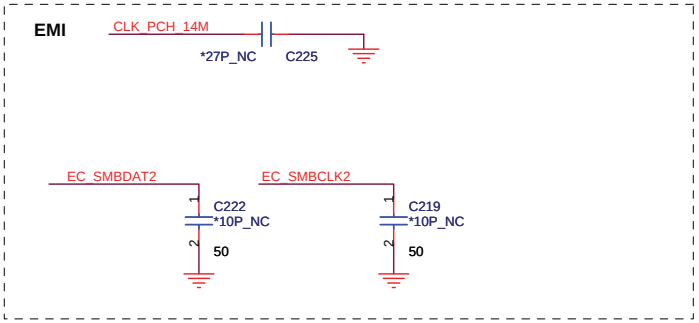
Quanta Computer Inc.

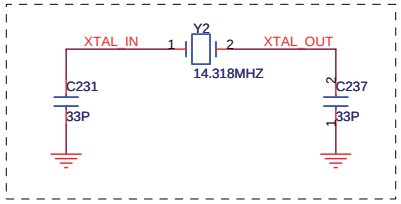
Project Name: XM2

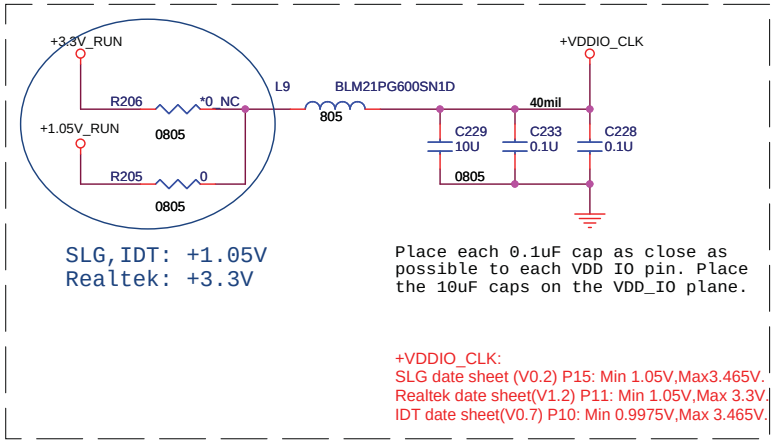
Title: MB Block Diagram		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 1 of 40	

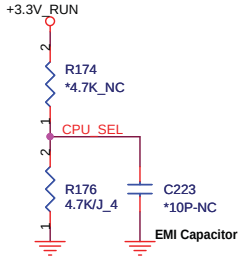


Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs









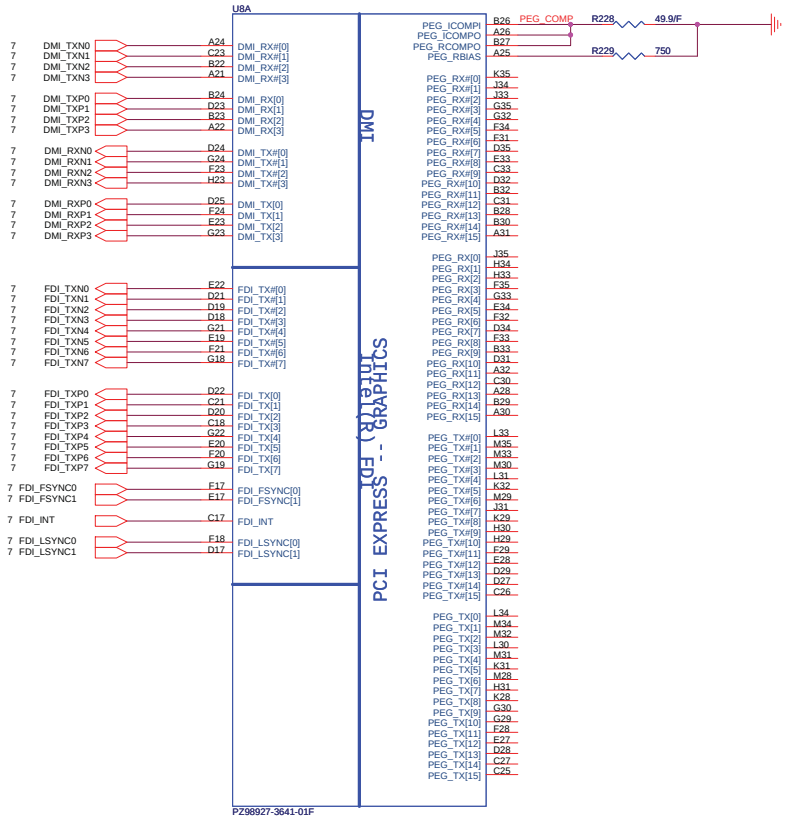
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

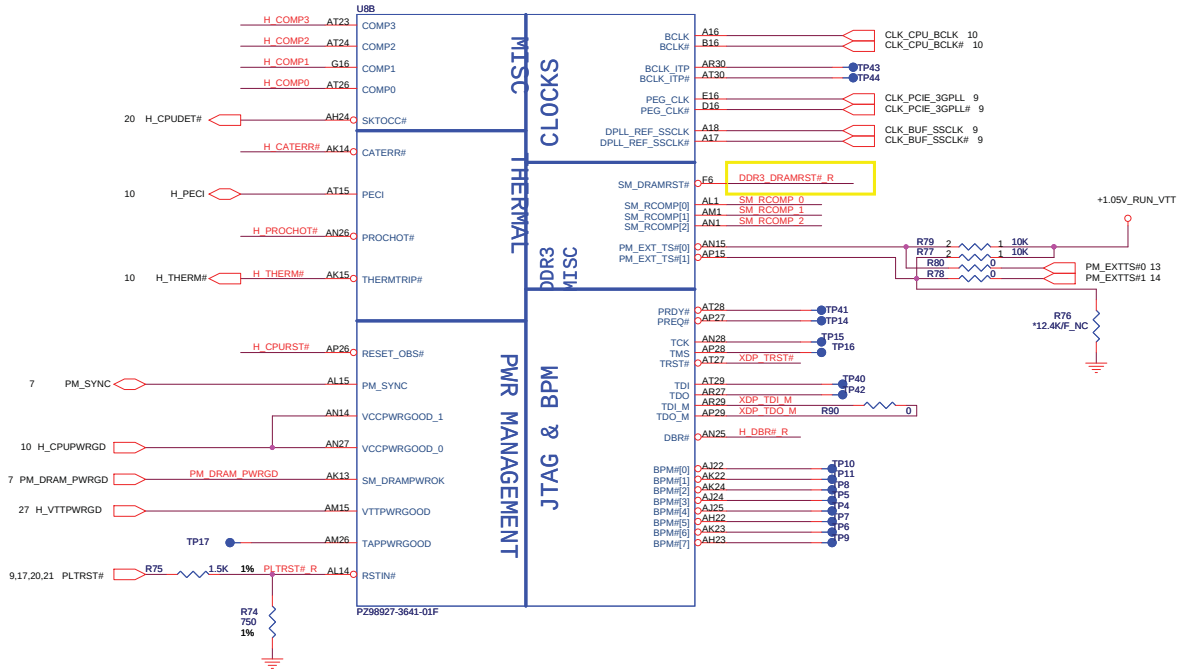
Quanta Computer Inc.
Project Name: GM7B

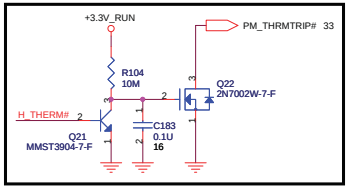
Title: Clock Gen		
Size	Document Number: GM7B	Rev: D
Date: Friday, January 15, 2010	Sheet 2 of 40	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

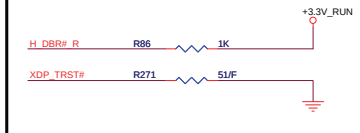


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

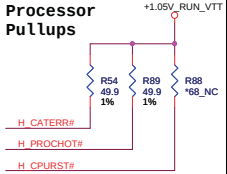




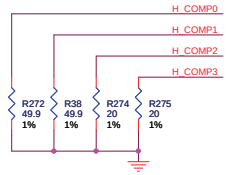
JTAG MAPPING



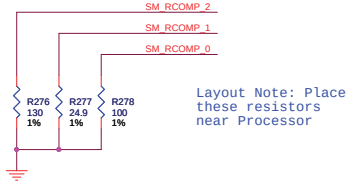
Processor Pullups



Processor Compensation Signals

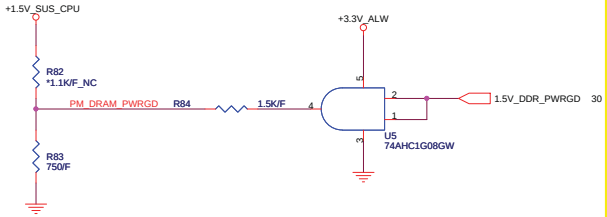


DDR3 Compensation Signals



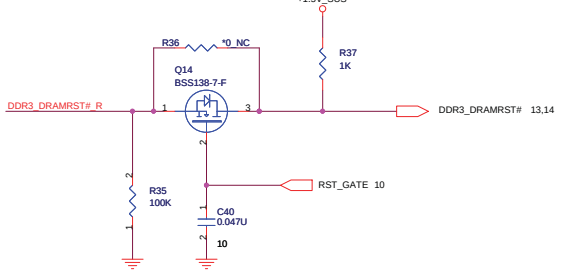
Layout Note: Place these resistors near Processor

S3 Power reduce



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

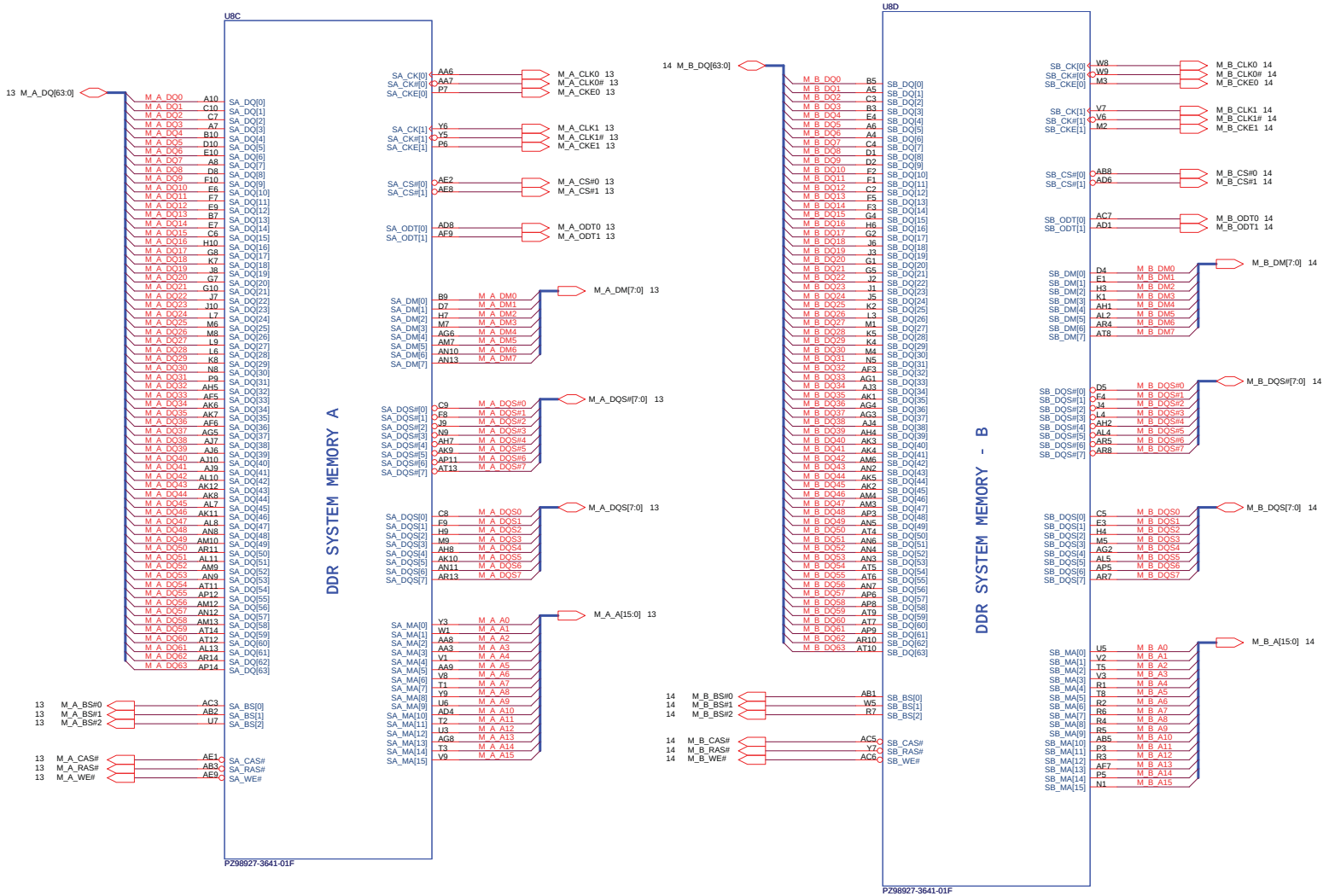
S3 Power reduce



Quanta Computer Inc.
Project Name: XM2

Title	CPU 1/4(PEG_DMI)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 3 of 40	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.
Project Name: XM2

Title	CPU 2/4(DDR)	
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 4 of 40	

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

AUBURNDALE PROCESSOR (POWER)

Note:
Place A and B near CPU
Route VCCSENSE and VSSENSE trace at 27.4 ohms, 7 mils spacing.

Note:
For Validating IMVP VR R483 should be STUFF and R2N1 NO_STUFF

S3 Power reduce

S3 Power reduce

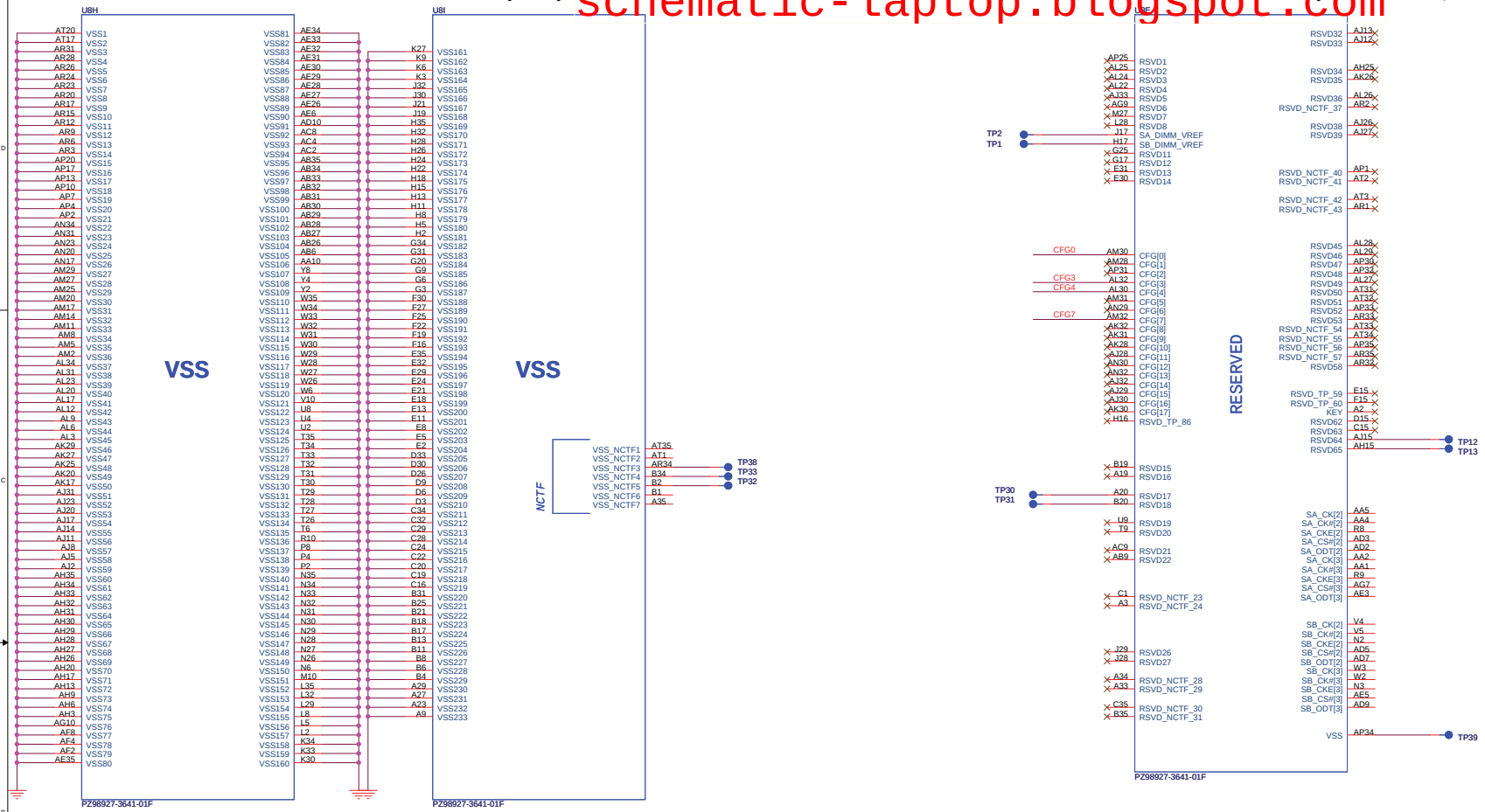
Q17 FDMS7670

Q19 BSS138-7-F

Quanta Computer Inc.	
Project Name: XM2	
Title: CPU 3/4(POWER)	
Size:	Document Number: XM2_MB Rev: D
Date: Friday, January 15, 2010	Sheet 5 of 40

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarksfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD

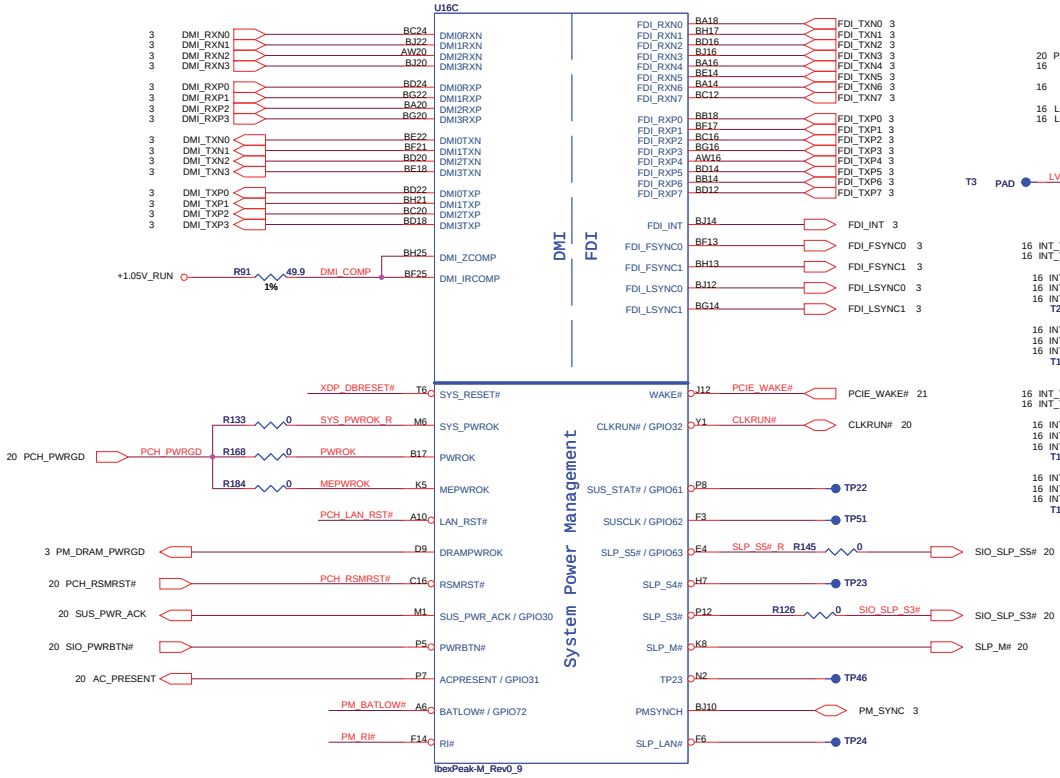
Quanta Computer Inc.
Project Name: XM2

Title: CPU 4/4(GND_RESV)

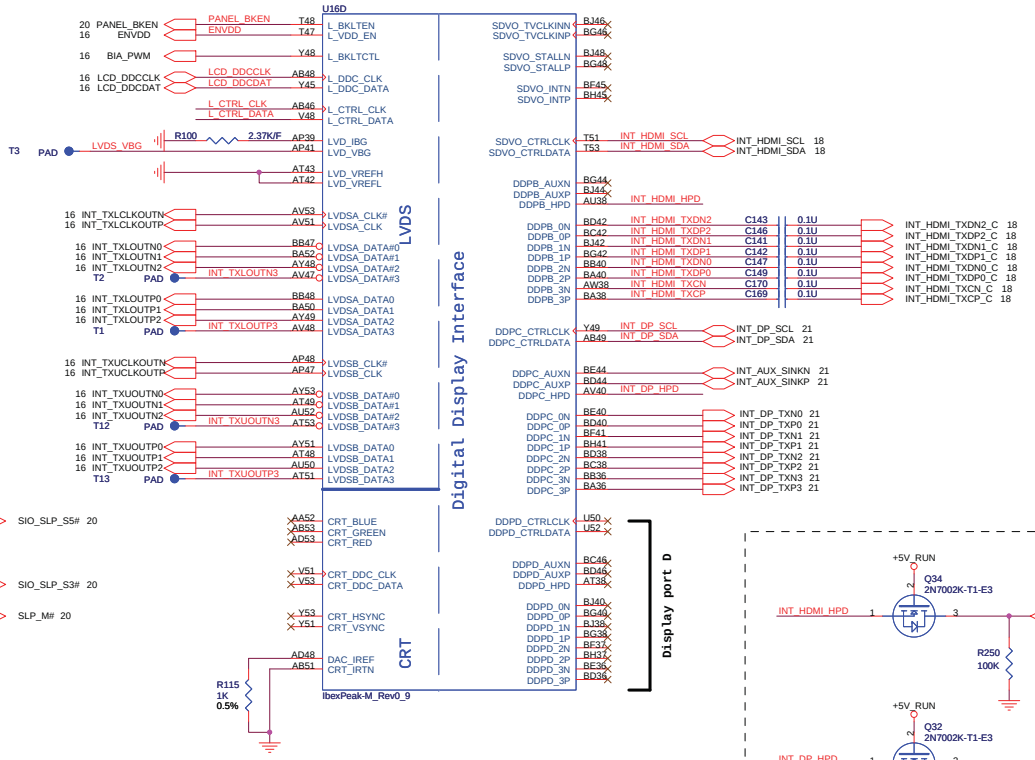
Size | Document Number: XM2_MB | Rev: D

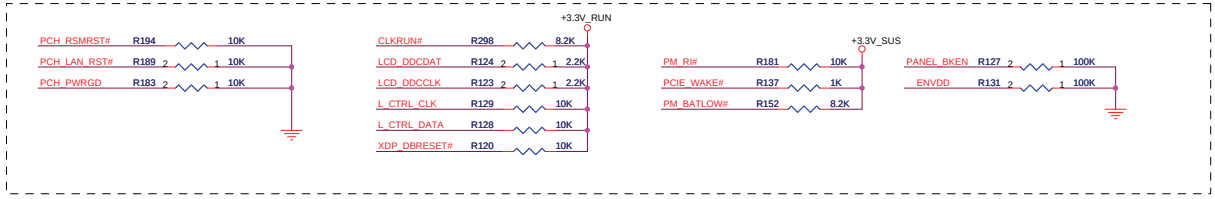
Date: Friday, January 15, 2010 | Sheet 6 of 40

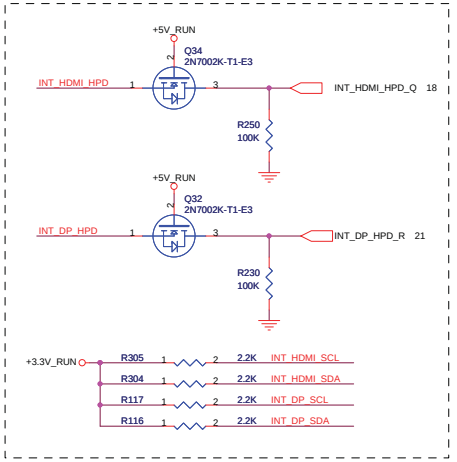
IBEX PEAK-M (DMI,FDI,GPIO)

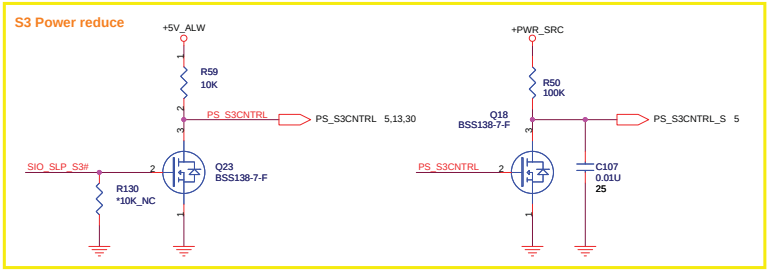


IBEX PEAK-M (LVDS,DDI)









Quanta Computer Inc.	Project Name: XM2	
Title: PCH 1/6 (DMI_VIDEO)		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 7 of 40	

IBEX PEAK-M (HDA,JTAG,SATA)

+3.3V_RUN
R308 *8.2K_NC SPKR

No Reboot Strap	
SPKR	Low=Default
	High=No Reboot

+RTC_CELL
R193 20K
R197 20K
C226 1uF
C227 1uF
R185 1M

Cap values depend on Xtal
C217 18PF
C218 18PF
W1 32.768KHZ
R157 10M

RTC_X1 B13
RTC_X2 D13
RTC_RST# C14
SRTC_RST# D17
SM_INTRUDER# A16
+RTC_CELL R192 330K PCH_INVRMEN A14

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

21 ICH_AZ_CODEC_BITCLK R159 33 ACZ_BIT_CLK
C216 *27P_NC
21 ICH_AZ_CODEC_SYNC R170 33 ACZ_SYNC
20,21 ICH_AZ_CODEC_RST# R160 33 ACZ_RST#
21 ICH_AZ_CODEC_SDOUT R169 33 ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

0 ohm resistor within 0.5 inch of pin

U16A

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0 / LAD0 D33, FWH1 / LAD1 B33, FWH2 / LAD2 C32, FWH3 / LAD3 A32, FWH4 / LFRAME# C34, LDRQ0# A34, LDRQ1# / GPIO23 F34, SERIRQ AB9
IHDA: ACZ_BIT_CLK A30, ACZ_SYNC D29, SPKR P1, ACZ_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, ACZ_SDOUT B29
SATA: HDA_DOCK_EN# / GPIO33 H32, HDA_DOCK_RST# / GPIO13 J30, SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9, SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8, SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6, SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5, SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO AF16, SATAICOMPI AF15, SATALED# T3, SATA0GP / GPIO21 Y9, SATA1GP / GPIO19 V1
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, JTAG_RST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1
IbexPeak-M_Rev0_9

21 SPKR
21 ICH_AZ_CODEC_SDIN0
TP26 TP28 TP27
20 PCH_GPIO33
24 KB_LED_DET
PCH_JTAG_TCK_BUF
PCH_JTAG_TMS TP47
PCH_JTAG_TDI TP48
PCH_JTAG_TDO TP50
PCH_JTAG_RST# TP49
Layout need to place at the same side of PCB
19 SPI_CLK
19 SPI_CS0#
TP45
19 SPI_SI
19 SPI_SO

FWH0 / LAD0 D33 → LPC_LAD0 20,21
FWH1 / LAD1 B33 → LPC_LAD1 20,21
FWH2 / LAD2 C32 → LPC_LAD2 20,21
FWH3 / LAD3 A32 → LPC_LAD3 20,21
FWH4 / LFRAME# C34 → LPC_LFRAME# 20,21
LDRQ0# A34 → TP29
LDRQ1# / GPIO23 F34 → TP25
SERIRQ AB9 → IRQ_SERIRQ 20

HDD: SATA0RXN AK7 → SATA_RX0- 23; SATA0RXP AK6 → SATA_RX0+ 23; SATA0TXN AK11 → SATA_TX0- 23; SATA0TXP AK9 → SATA_TX0+ 23
ODD: SATA1RXN AH6 → SATA_RX1- 23; SATA1RXP AH5 → SATA_RX1+ 23; SATA1TXN AH9 → SATA_TX1- 23; SATA1TXP AH8 → SATA_TX1+ 23
eSATA: SATA4RXN AD9 → ESATA_ITX_DRX_N4 21; SATA4RXP AD8 → ESATA_ITX_DRX_P4 21; SATA4TXN AD6 → ESATA_IRX_DTX_N4_C 21; SATA4TXP AD5 → ESATA_IRX_DTX_P4_C 21
HDD2: SATA5RXN AD3 → SATA_RX5- 23; SATA5RXP AD1 → SATA_RX5+ 23; SATA5TXN AB3 → SATA_TX5- 23; SATA5TXP AB1 → SATA_TX5+ 23

SATAICOMPO AF16
SATAICOMPI AF15 — SATAICOMPO — R105 37.4 1% — +1.05V_RUN
Close to PCH <500mil

SATALED# T3 → R303 10K → +3.3V_RUN; SATA_ACT# 25
SATA0GP / GPIO21 Y9 → R112 10K → +3.3V_RUN
SATA1GP / GPIO19 V1 → R301 10K → +3.3V_RUN

R310 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled

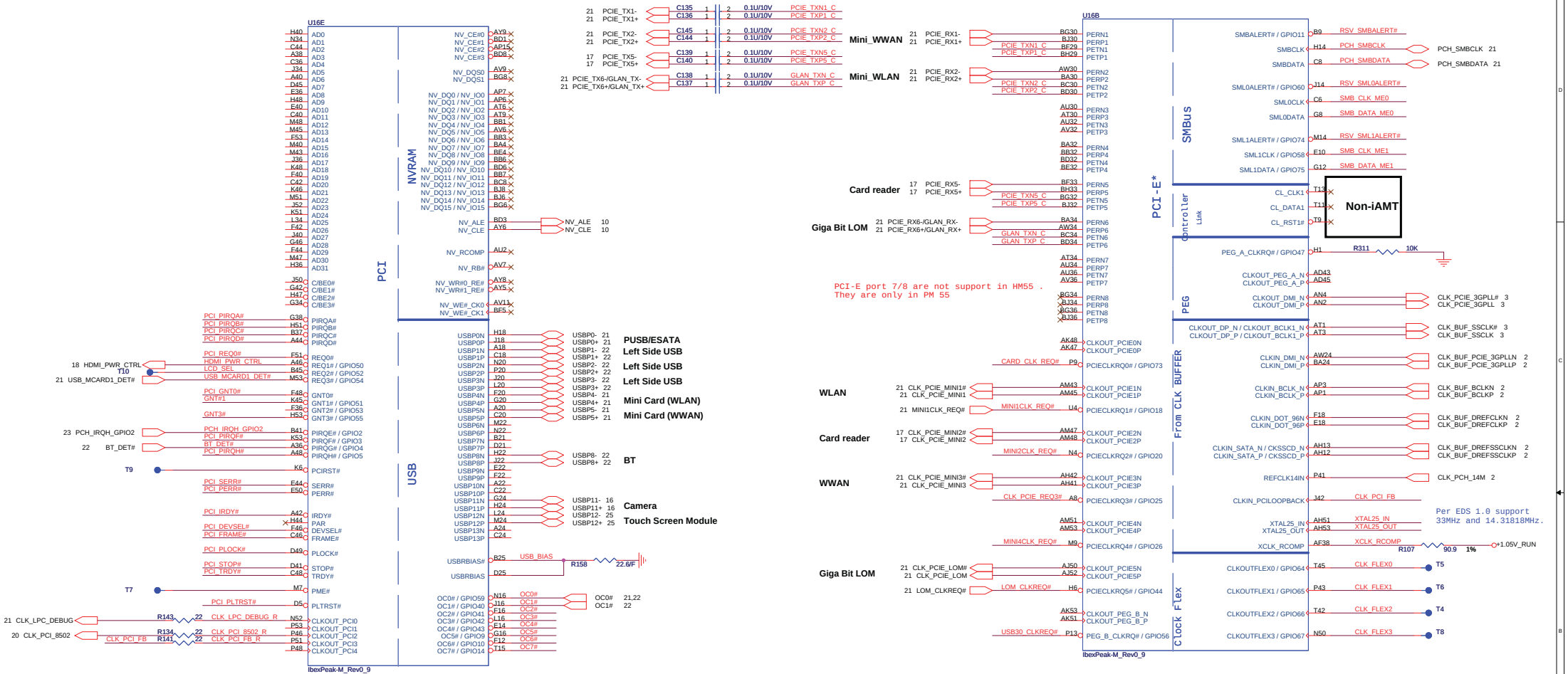
R136 *1K_NC PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

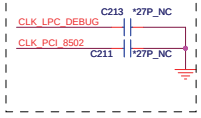
Quanta Computer Inc.
Project Name: XM2
Title: PCH 2/6 (SATA_SPI)
Size: Document Number: XM2_MB Rev: D
Date: Friday, January 15, 2010 Sheet 8 of 40

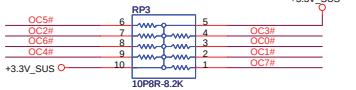
IBEX PEAK-M (PCI,USB,NVRAM)

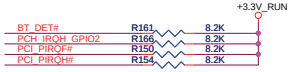
IBEX PEAK-M (PCI-E,SMBUS,CLK)

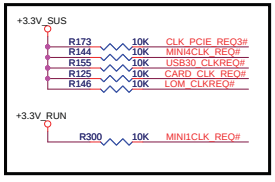


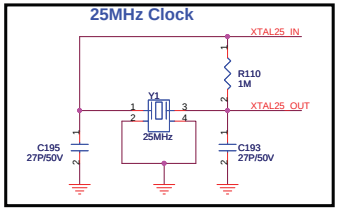
Reserve capacitor pads for improving WWAN.

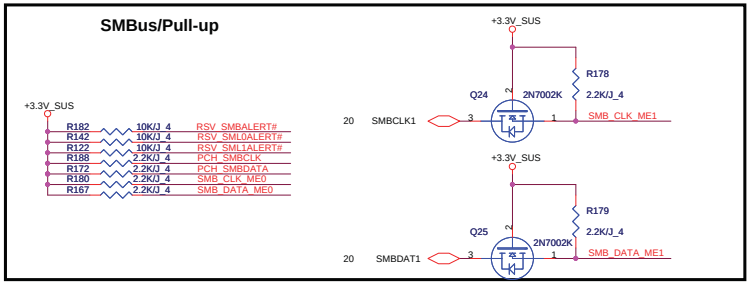


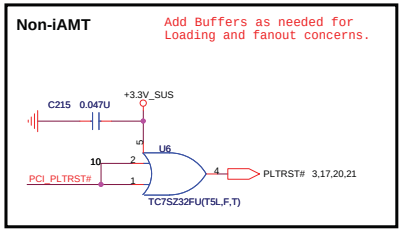


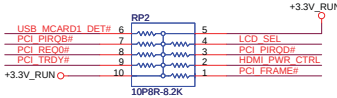


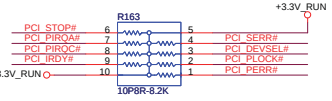


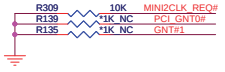






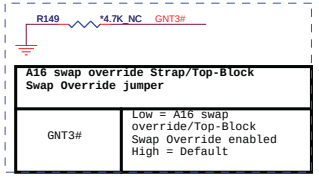






Boot BIOS Strap

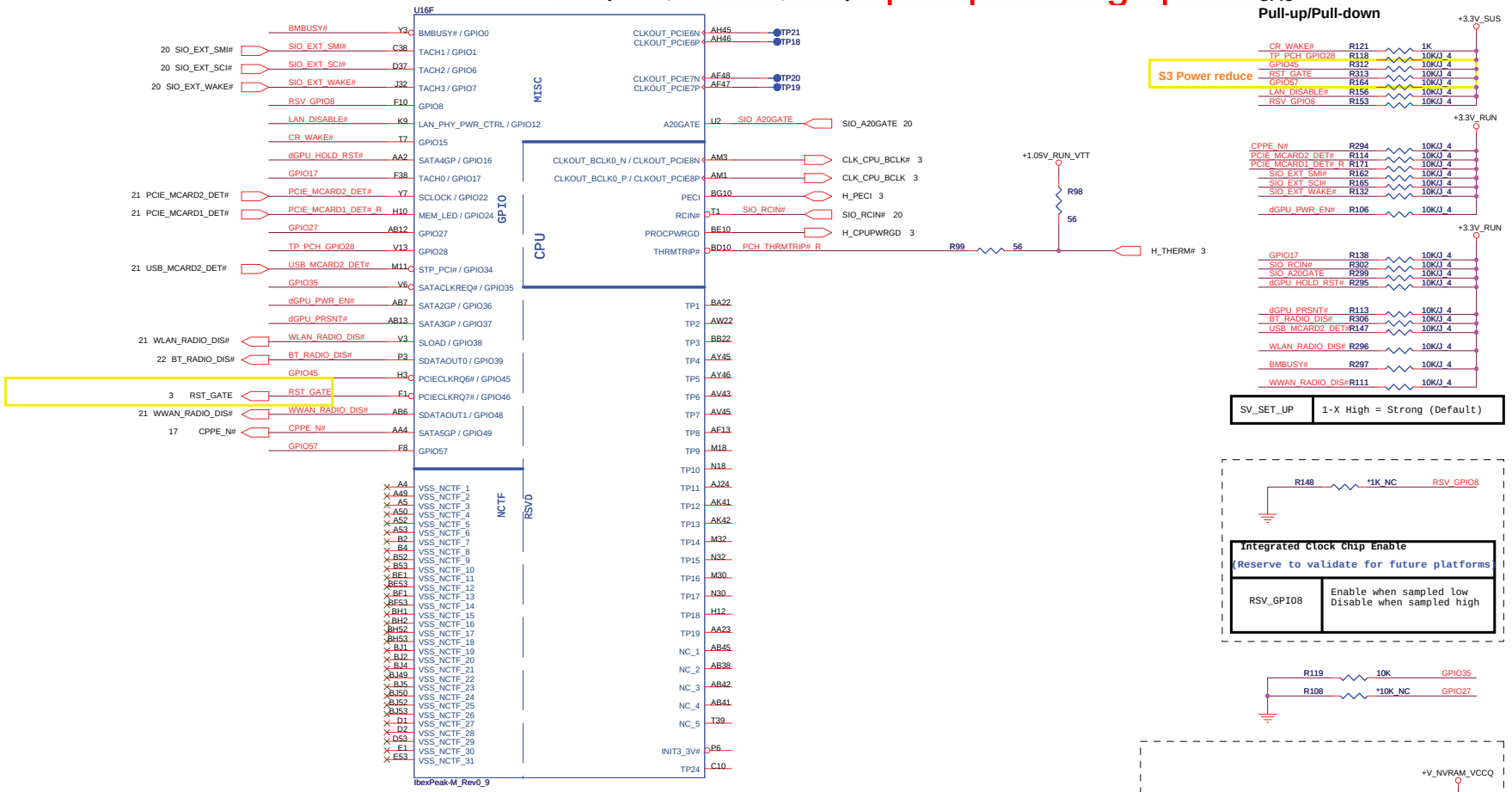
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Quanta Computer Inc.
Project Name: XM2

Title	PCH 3/6 (PCI_SMBUS_CLK)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 9 of 40	

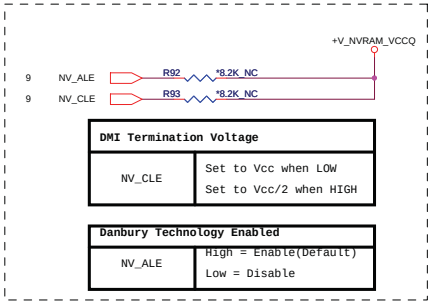
IBEX PEAK-M (GPIO,MISC,NCTF,RSVD)



GPIO Pull-up/Pull-down

S3 Power reduce

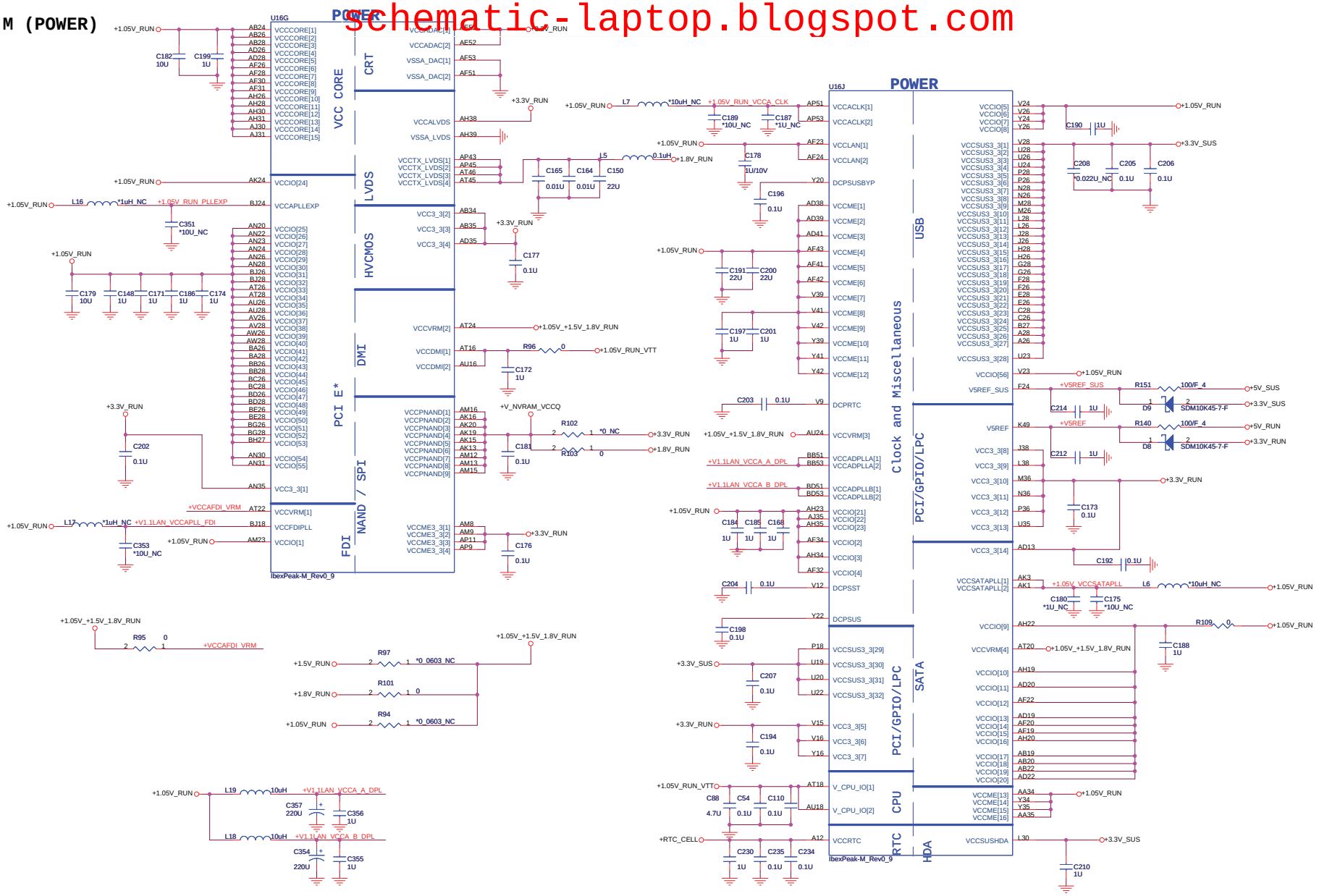
SV_SET_UP	1-X High = Strong (Default)



Quanta Computer Inc.
Project Name: XM2

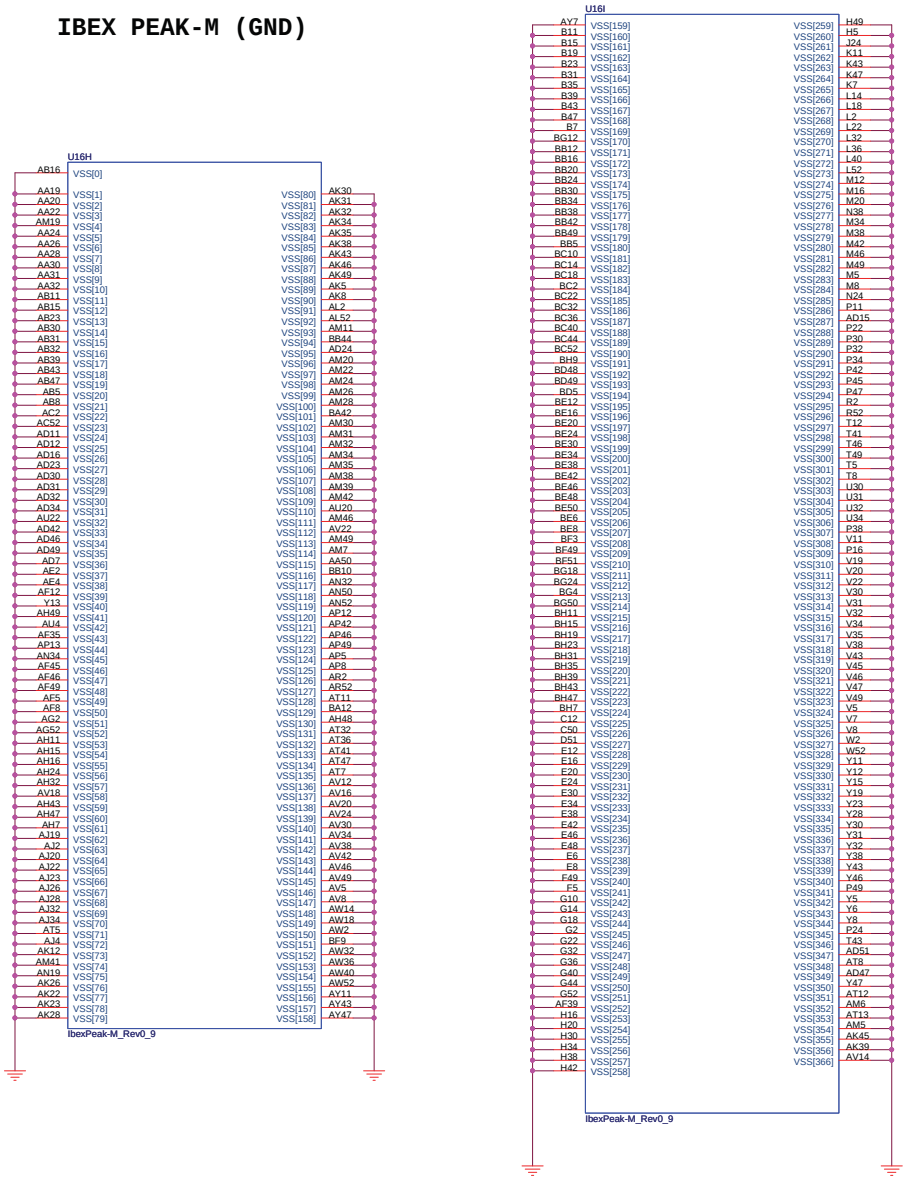
Title	PCH 4/6 (GPIO)	
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 10 of 40	

IBEX PEAK-M (POWER)



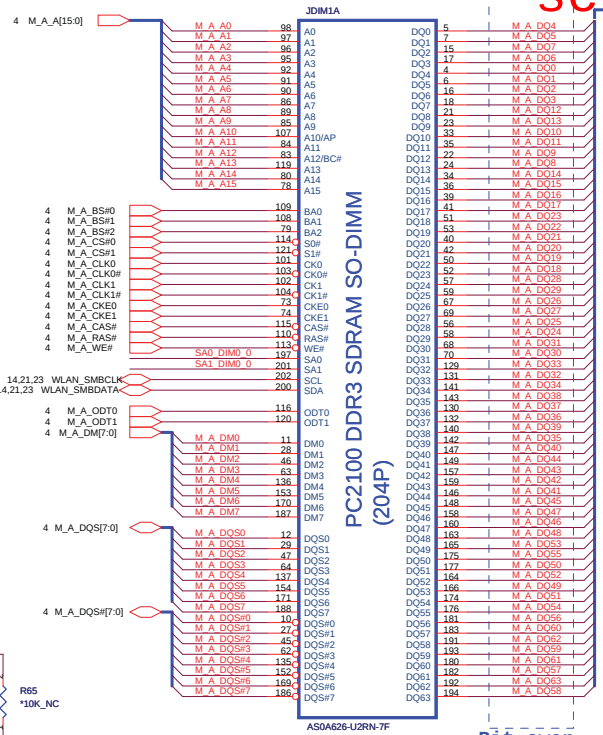
Quanta Computer Inc.
Project Name: XM2
Title: PCH 5/6 (POWER)
Size: Document Number: XM2_MB
Rev: D
Date: Friday, January 15, 2010
Sheet 11 of 40

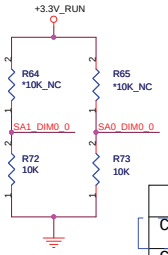
IBEX PEAK-M (GND)



Quanta Computer Inc.		
Project Name: XM2		
Title: PCH 6/6 (GND)		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 12 of 40	

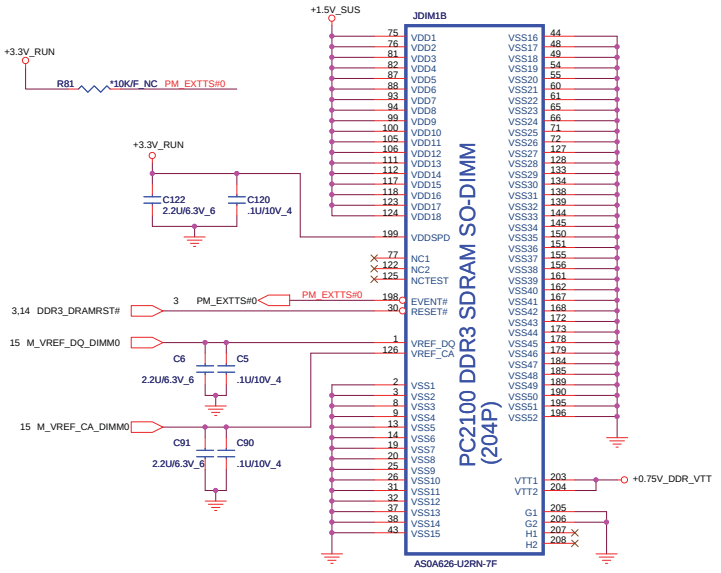
CHA_DIMM0_SO_SIDE

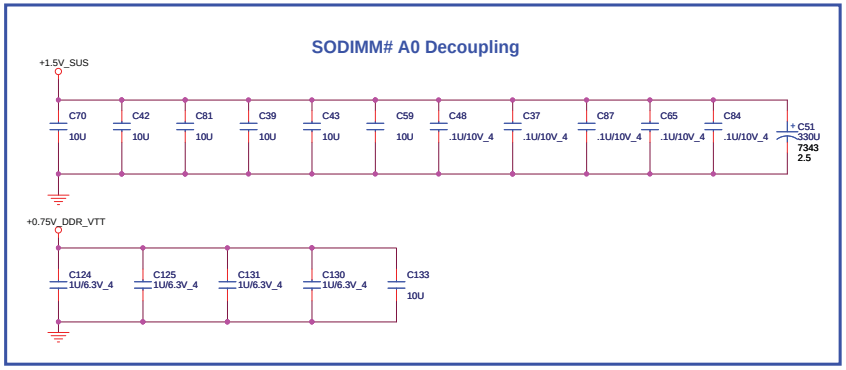


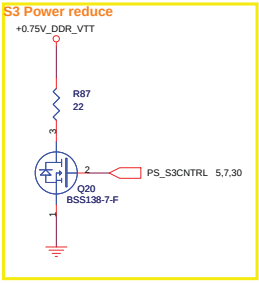


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



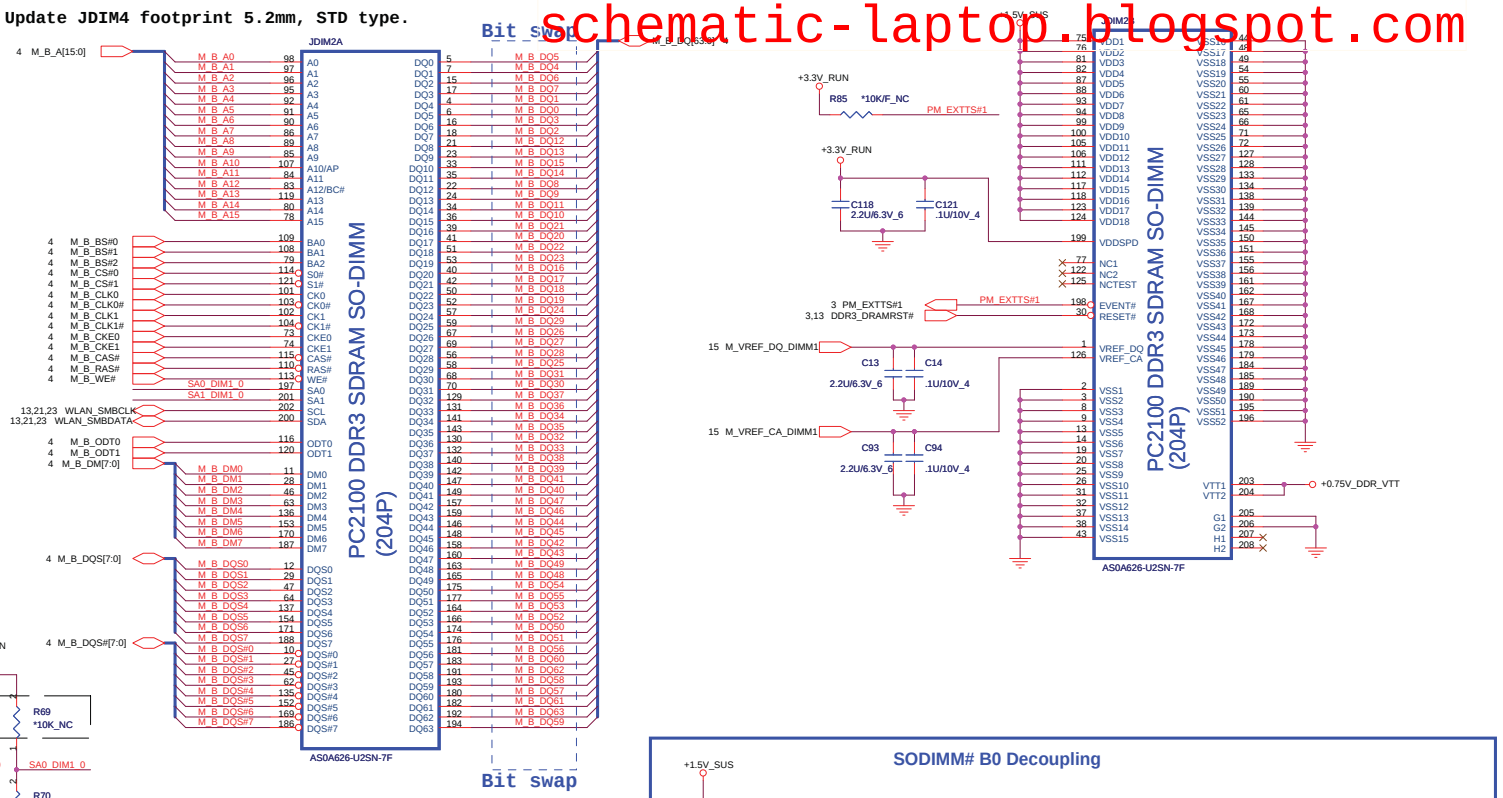


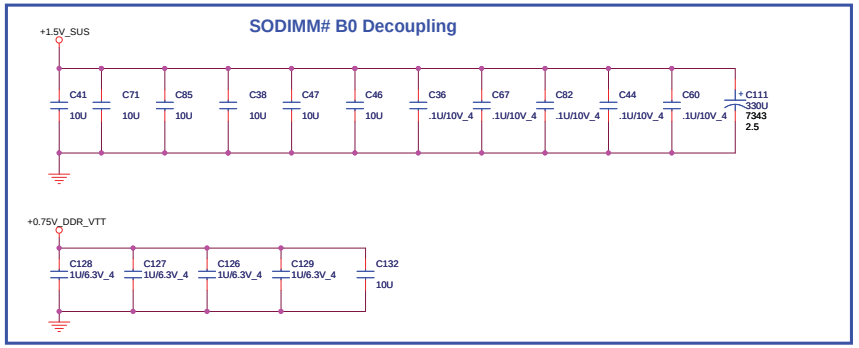


Quanta Computer Inc.
Project Name: XM2

Title	DDR3 DIMM-A0		
Size	Document Number XM2_MB		Rev D
Date: Friday, January 15, 2010	Sheet 13 of 40		

0105CT: Update JDIM4 footprint 5.2mm, STD type.



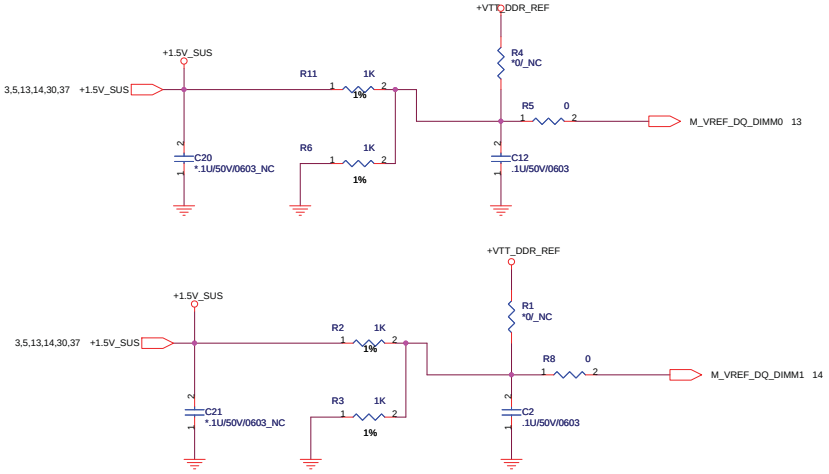


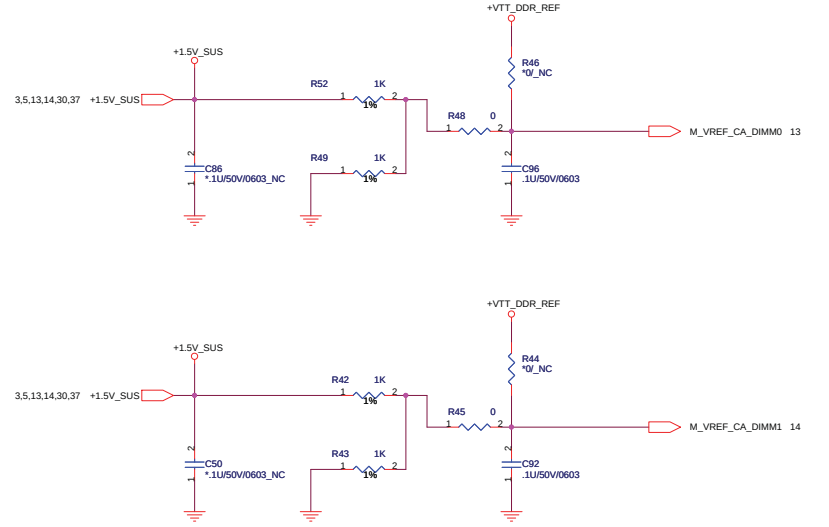
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

Quanta Computer Inc.	
Project Name: XM2	
Title: DDR3 DIMM-B0	
Size	Document Number: XM2_MB — Rev: D
Date: Friday, January 15, 2010	Sheet 14 of 40

Fixed SO-DIMM VREF_DQ (M1): Default

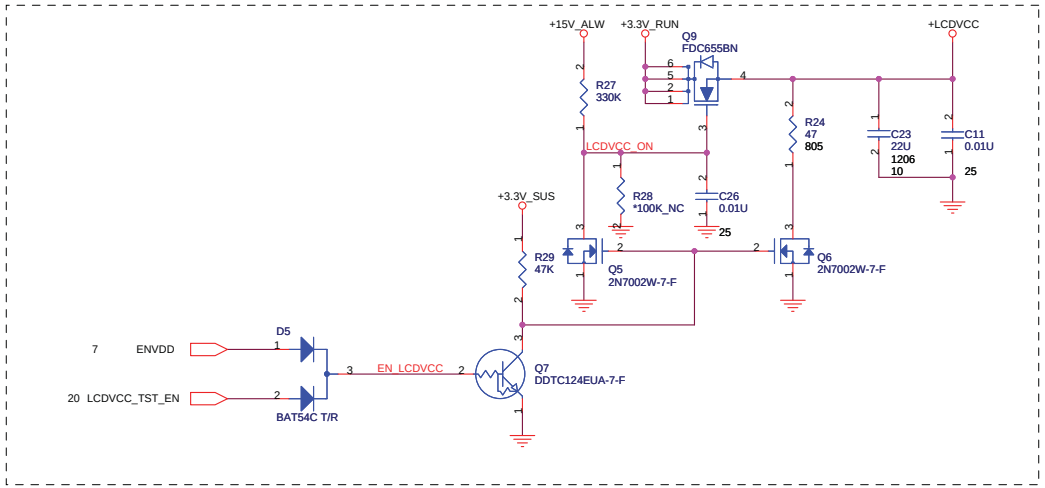


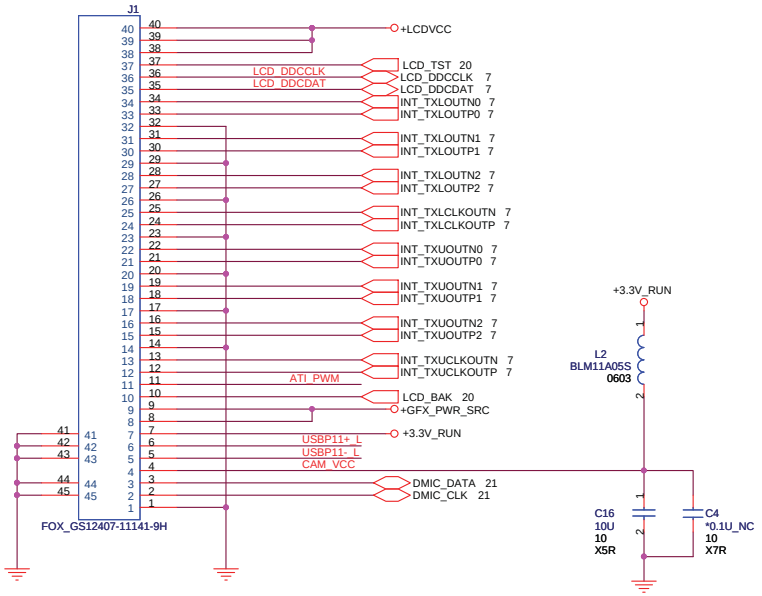


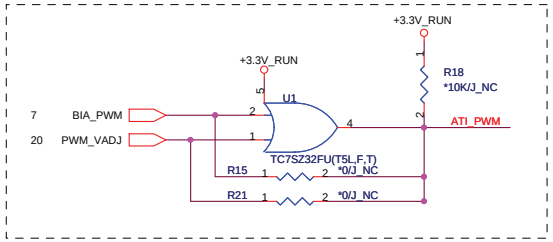
Quanta Computer Inc.
Project Name: XM2

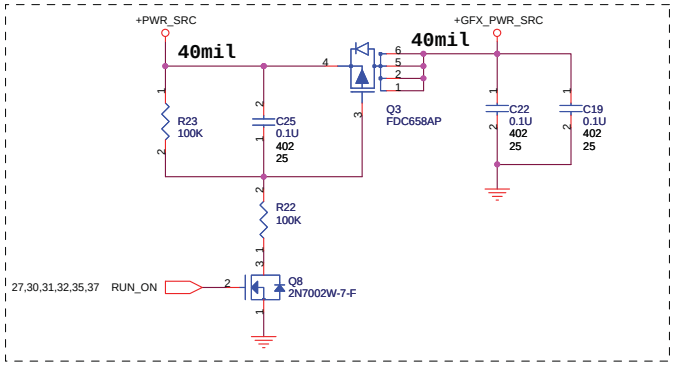
Title	DDR3 VREF	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 15 of 40	

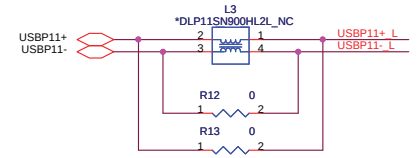
40Pin LVDS & Array Microphone & Camera Connector

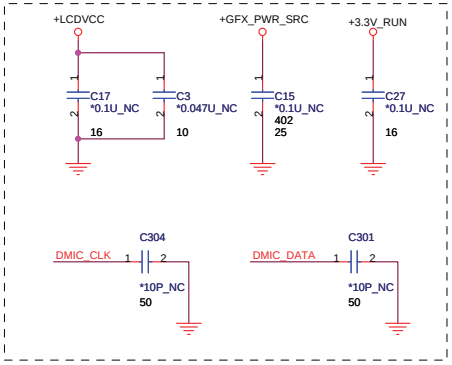












Quanta Computer Inc.

PROJECT : Calpella UMA

Size	Document Number	Rev
	LVDS CONN	1A

Date: Friday, January 15, 2010 Sheet 16 of 40

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

+DVDD18 +APVDD R323 0 0603 (>40mil)

+3.3V_RUN +VDD33 R321 0 0603 (>40mil)

(>20mil) +CR_PWR R322 0 0603 +3.3V_CARD C368 22U/6.3V_8 C284 0.1U

+DVDD18 C372 0.1U C375 0.1U

+VDD33 C373 0.1U C369 0.1U

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

+3.3V_CARD C283 2.2U/6.3V CC0603

C7577 need close to pin7

CON3 — TAS_5-250907001000-9 / 5in1-5-250907001000-9-45p

SD_MS_XD-D2, SD_MS_XD-D3, SD_MS_XD-D4, SD-CMD_MS-BS_XD-WE#, SD_MS_XD-D5, SD-CLK_MS-CLK_XD-CE#, SD_MS_XD-D3, MS_CD#, SD_MS_XD-D2, SD_MS_XD-D0, SD_MS_XD-D1, SD-CMD_MS-BS_XD-WE#, SD-CLK_MS-CLK_XD-CE#, SD_MS_XD-D6, SD_MS_XD-D7, SD_MS_XD-D0, SD_MS_XD-D1

SD-9(D2), SD-1(D3), MMC-10(D4), SD-2(SD_CMD), MMC-11(D5), SD-3(VSS), SD-4(VDD), MS-10(VSS), MS-9(VCC), MS-8(SCLK), MS-7(D3), MS-6(INS), MS-5(D2), MS-4(D0), MS-3(D1), MS-2(BS), MS-1(VSS), SD-5(CLK), MMC-12(D6), SD-6(GND), MMC-13(D7), SD-7(D0), SD-8(D1)

SD(SW.COM), SD(SW.CD), XD-1(GND), XD-0(CDSW), XD-2(R/-B), XD-3(RE), XD-4(CE), XD-5(CLE), XD-6(ALE), XD-7(WE), XD-8(-WP), XD-9(GND), XD-10(D0), XD-11(D1), XD-12(D2), XD-13(D3), XD-14(D4), XD-15(D5), XD-16(D6), XD-17(D7), XD-18(VCC), SD(SW.WP)

C281 270P/25V, C279 *10P_NC, C282 *10P_NC

+3.3V_CARD **C85 need close to pin44** C278 2.2U 6.3 X5R

SD_CD#, XD_CD#, XD-R/B#, XD-RE#, SD-CLK_MS-CLK_XD-CE#, XD-CLE, XD-ALE, SD-CMD_MS-BS_XD-WE#, SD-WP_XD-WP#, SD_MS_XD-D0, SD_MS_XD-D1, SD_MS_XD-D2, SD_MS_XD-D3, SD_MS_XD-D4, SD_MS_XD-D5, SD_MS_XD-D6, SD_MS_XD-D7, SD-WP_XD-WP#

C271 *270P/25V_NC

XD_CD# C285 *270P/25V_NC

SD_MS_XD-D1 R224 *0_NC C280 *10P_NC

+3.3V_CARD R327 10K SD-WP_XD-WP# R328 1K XD-R/B#

+3.3V_RUN R326 10K XD-CLE R325 200K XD-ALE

U17 JMB389

+VDD33, SD_MS_XD-D4, SD_MS_XD-D5, SD_MS_XD-D6, SD_MS_XD-D7, XD-RE#

TAV33, SPI_SI, SPI_SO, SPI_CSN, SPI_CLK, GND, SPI_SCK, MDIO8, MDIO9, MDIO10, MDIO11, MDIO12

+DVDD18, DV18, GND, TXIN, MDIO7, MDIO4, MDIO5, SDDV33_18, DV33, MDIO3, MDIO2, MDIO1, MDIO0

XD-CLE, SD-CMD_MS-BS_XD-WE# R324 22, SD-CLK_MS-CLK_XD-CE#, C374 22P/50V_4, +VDD33, C371 2.2U

SD_MS_XD-D3, SD_MS_XD-D2, SD_MS_XD-D1, SD_MS_XD-D0

MDIO6, MDIO13, MDIO14, CR1_LEDN, DV33, DV33, DV18, CR1_PCTLN, CR1_CD0N, CR1_CD1N, CR1_CD2N, CPPE_N

SD-WP_XD-WP#, XD-R/B#, XD-ALE, +VDD33, +CR_PWR, +DVDD18, SD_CD#, MS_CD#, XD_CD#, CPPE_N#_C

XRSTN, XTEST, APCLKN, APCLKP, APCVDD, APGND, APREXT, APRXP, APRXN, APV18, APTXN, APTXP

JMB389

MIDO Single End = 50 ohm

MIDO[0..5] Single Skew Should be smaller +/- 100 mil for SDA3.Application

+3.3V_SUS R319 *10K_NC CPPE_N# 10 Q47 *2N7002W-7-F_NC

C370 10U — Needs close to Pin18: 12mil/<250mil

3,9,20,21 PLTRST# R320 0 C367 0.1U 10 X7R

9 CLK_PCIE_MINI2# 9 CLK_PCIE_MINI2

R318 12K +APV18 PCIE_RXN5_C PCIE_RXP5_C

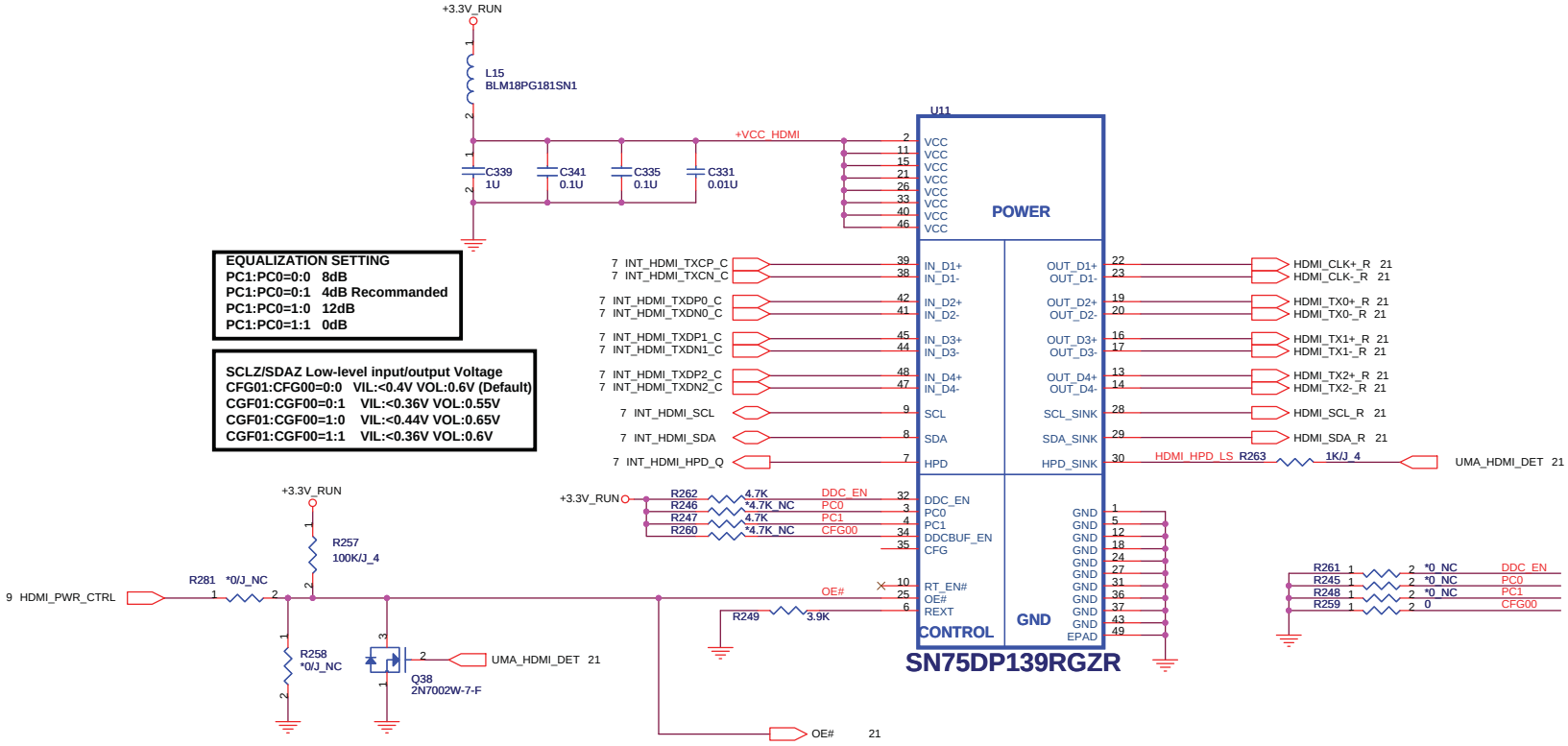
+APVDD (20mil) +APV18 +APVDD

C360 10U, C364 0.1U, C362 1000P, C363 0.1U, C361 10U

C365 0.1U, C366 0.1U

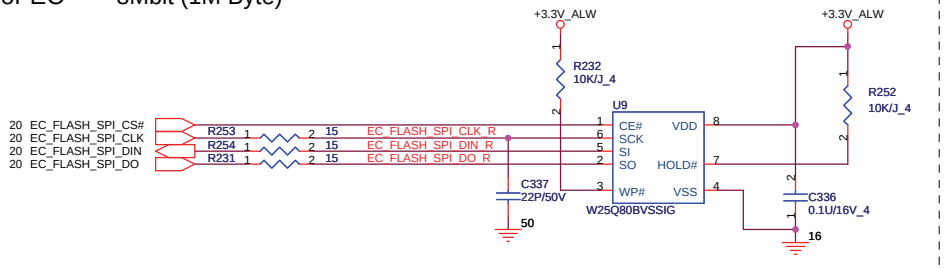
PCIE_TX5+ PCIE_TX5- PCIE_RX5- PCIE_RX5+

Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: Card Reader (JMB389A)	Rev 1A
Date: Friday, January 15, 2010	Sheet 17 of 40	

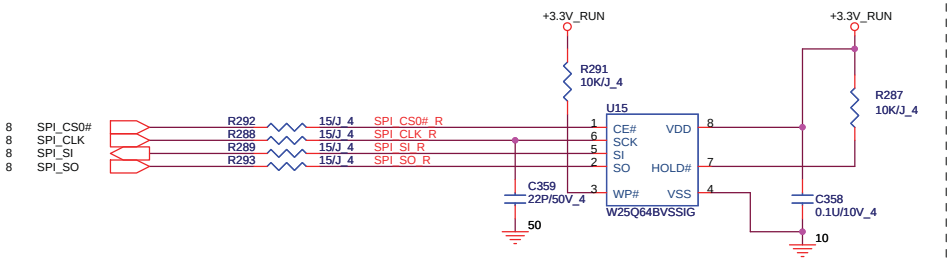


Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: HDMI CONN	Rev: 1A
Date: Friday, January 15, 2010	Sheet 18 of 40	

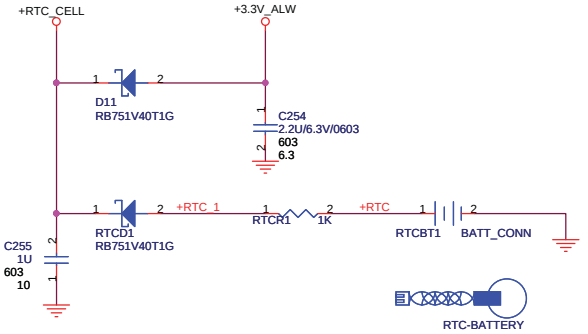
For EC 8Mbit (1M Byte)



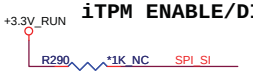
For PCH 64Mbit (8M Byte), SPI



RTC BATTERY



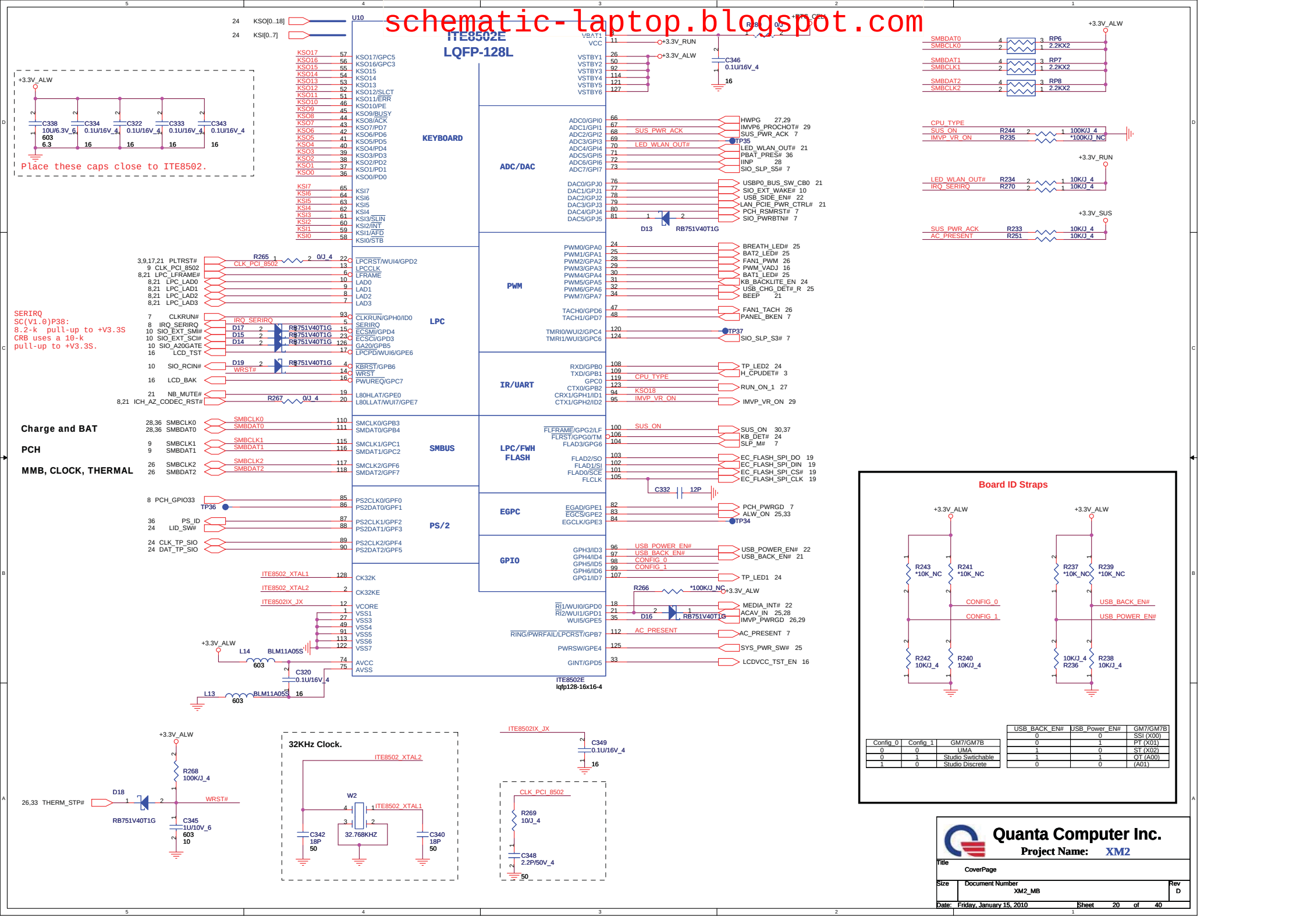
iTPM ENABLE/DISABLE

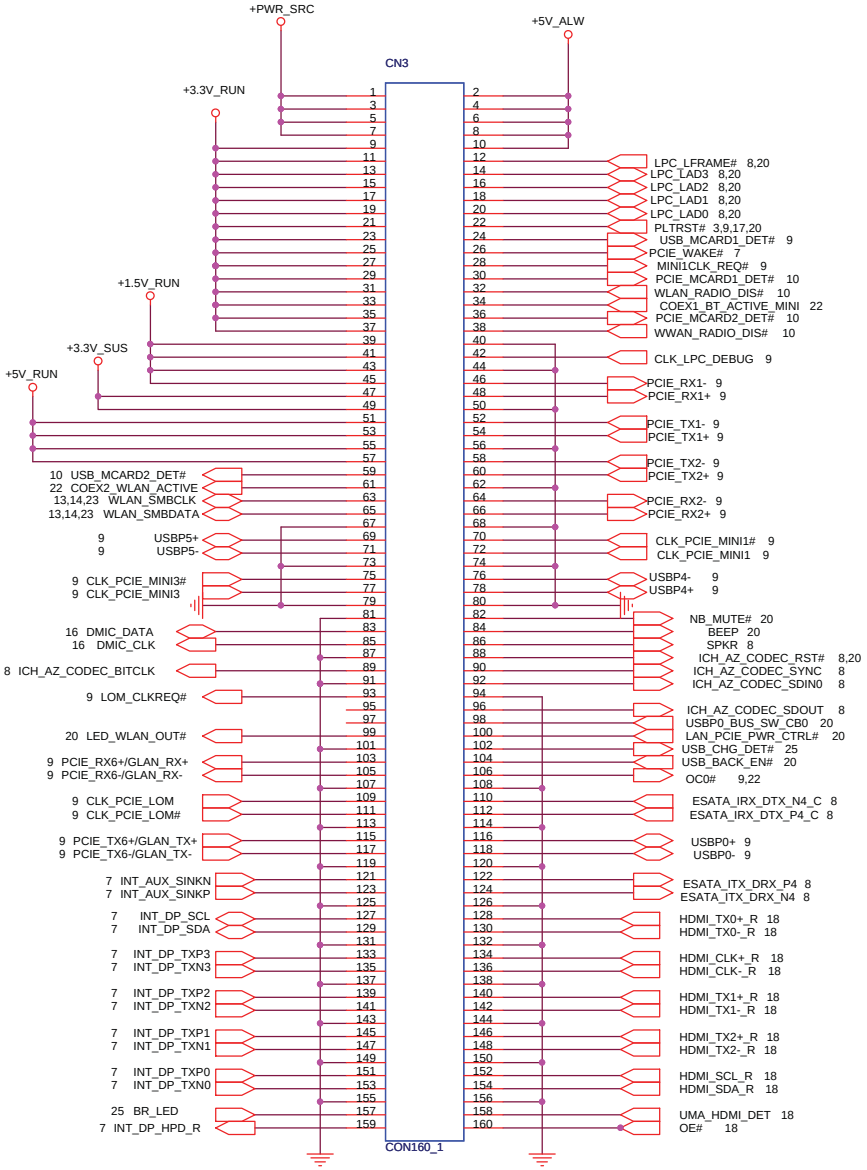


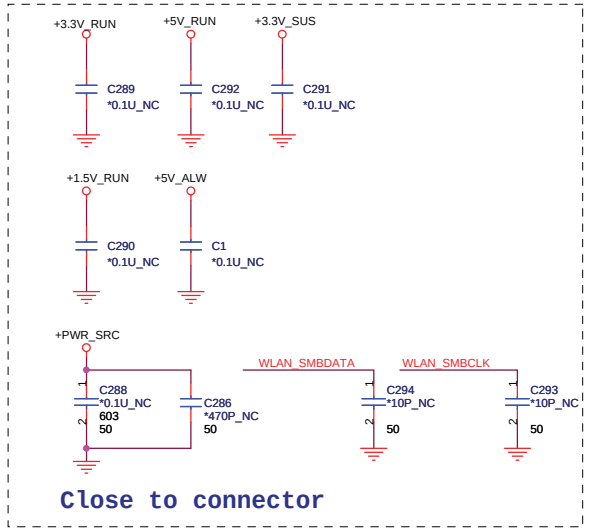
TPM Function	R712
Enable	Mount
Disable	NC (Default)

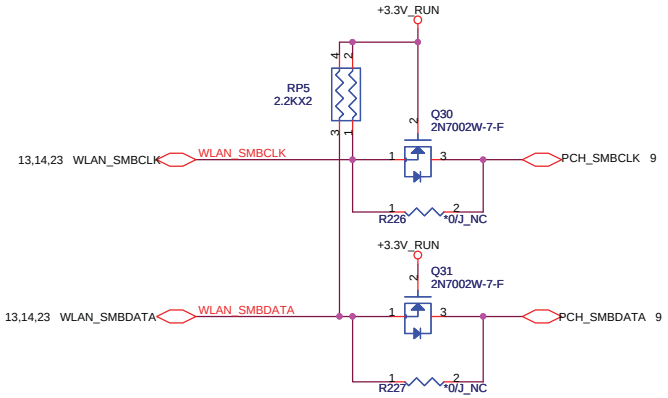
Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	FLASH / RTC	1A
Date: Friday, January 15, 2010	Sheet 19 of 40	





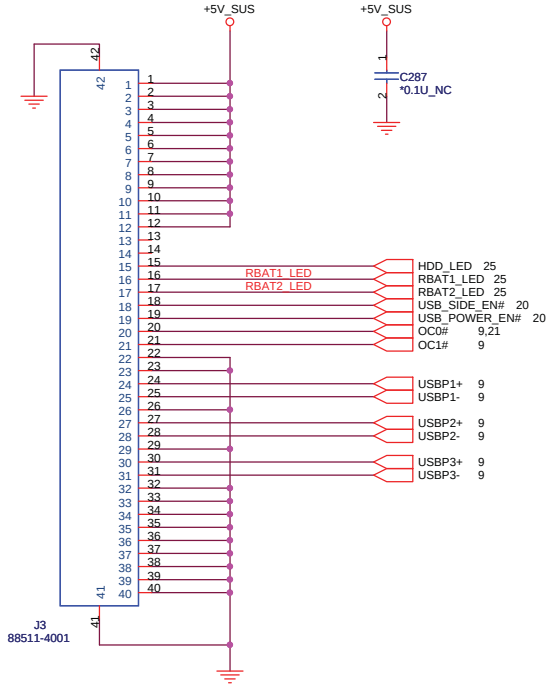




Quanta Computer Inc.
PROJECT : Calpella UMA

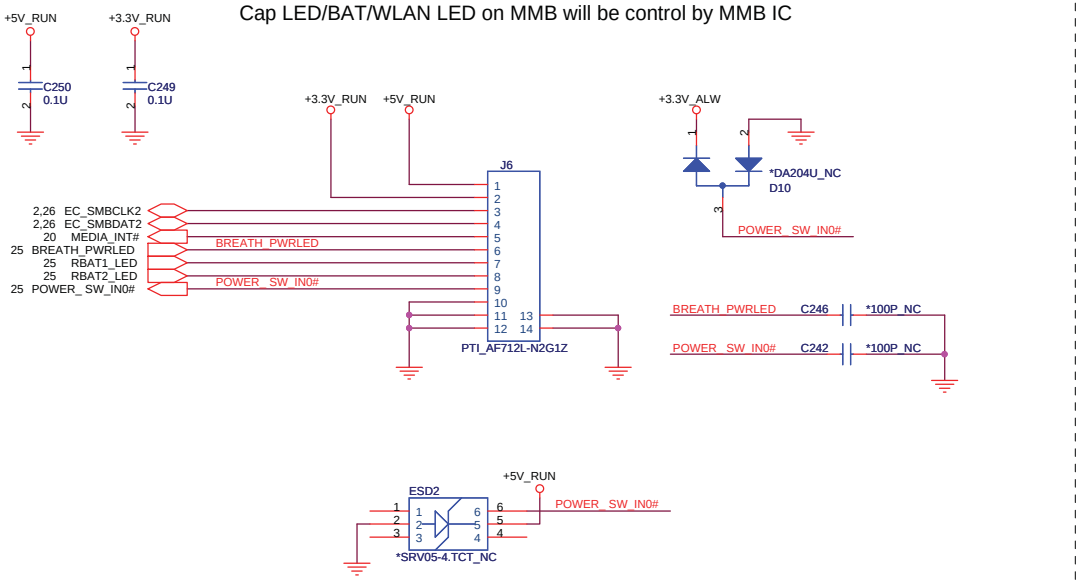
Size	Document Number	Rev
	MB CODE (WLAN/WPAN)	1A
Date: Friday, January 15, 2010	Sheet 21 of 40	

USB IO 40 pins

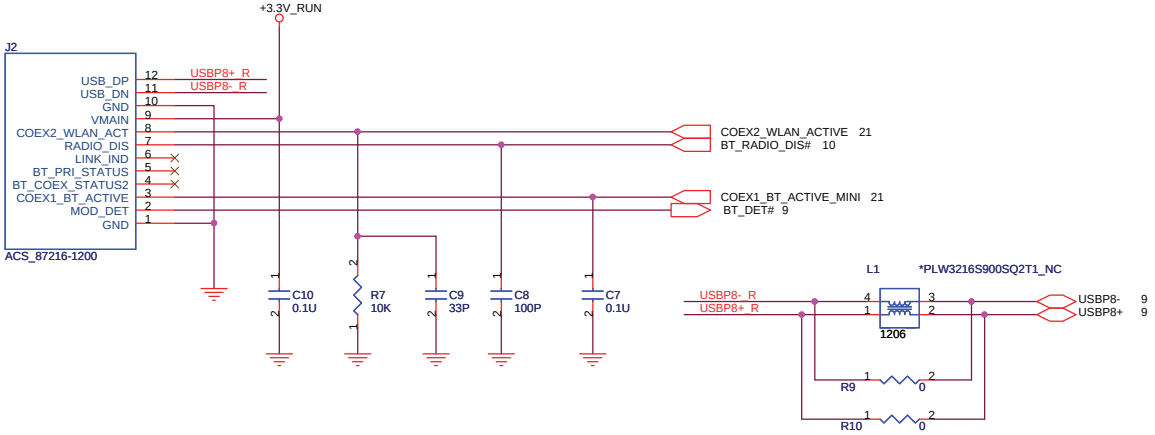


MMB & Power Board 12pins

Cap LED/BAT/WLAN LED on MMB will be control by MMB IC

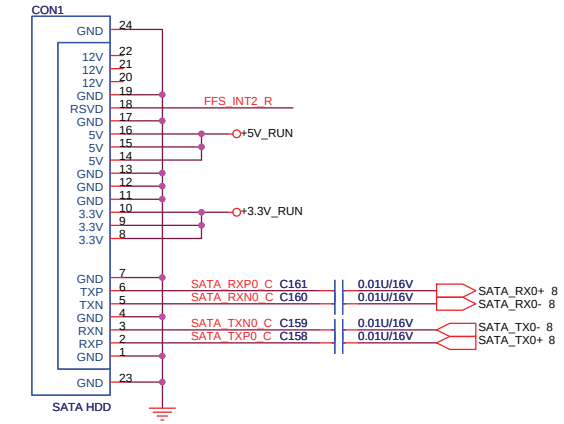


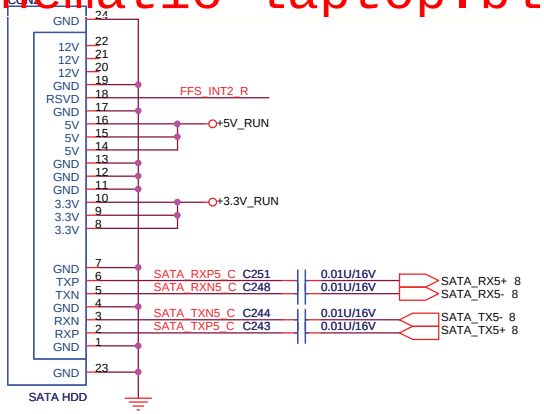
Support Dell BT3xx series module
Bluetooth WTB Conn

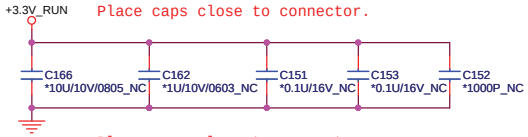


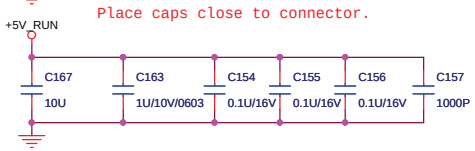
Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: Left USB / MMB CONN	Rev: 1A
Date: Friday, January 15, 2010	Sheet 22 of 40	

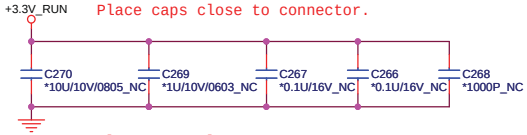
SATA Connector.

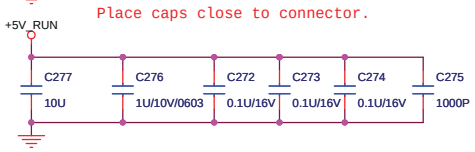




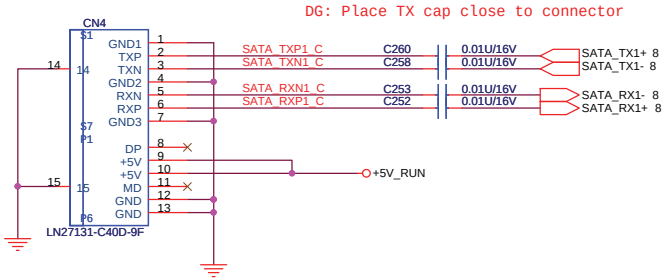


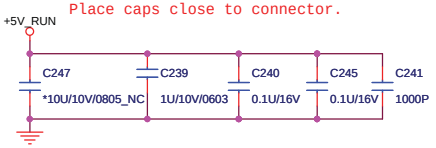




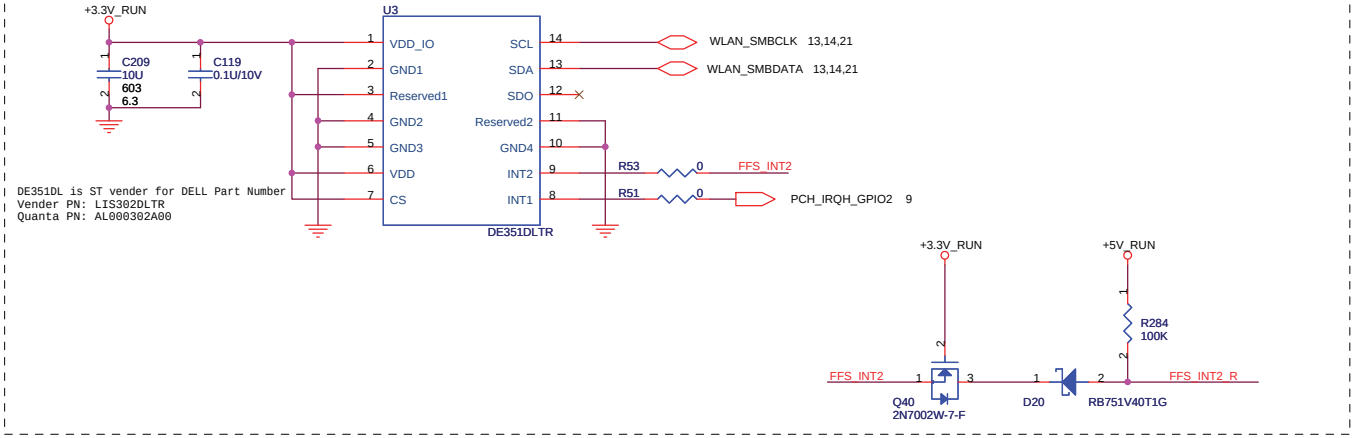


ODD Connector





3-axis Fall Sensor (HDD data protector)



Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	SATA (HDD&ODD)	1A
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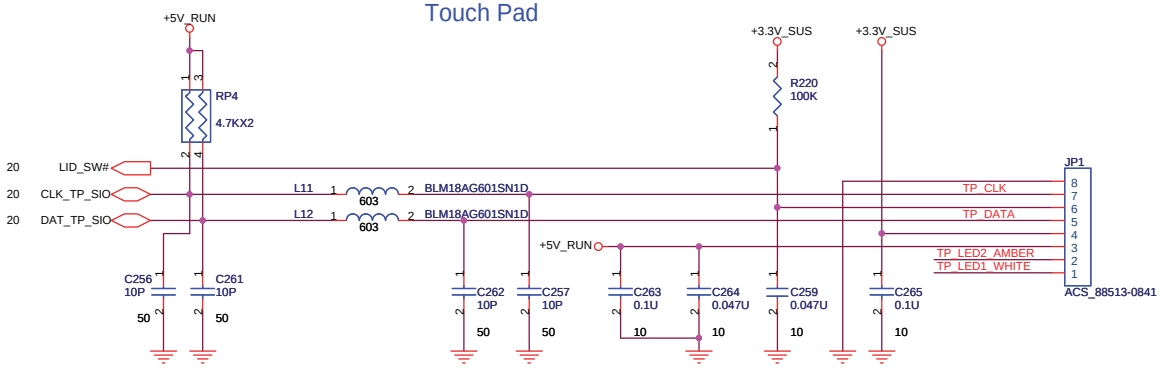
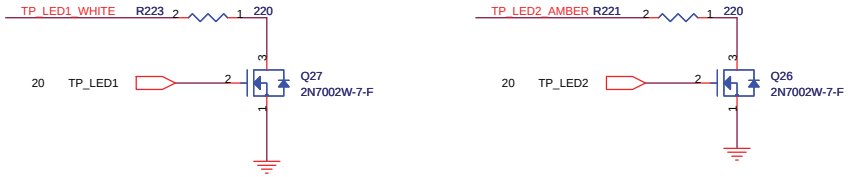
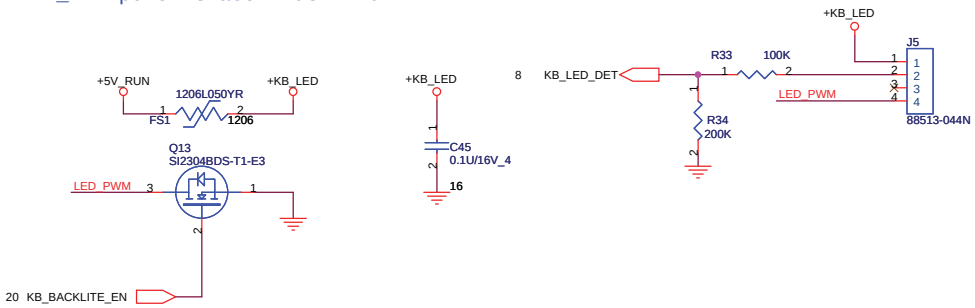
Touch Pad



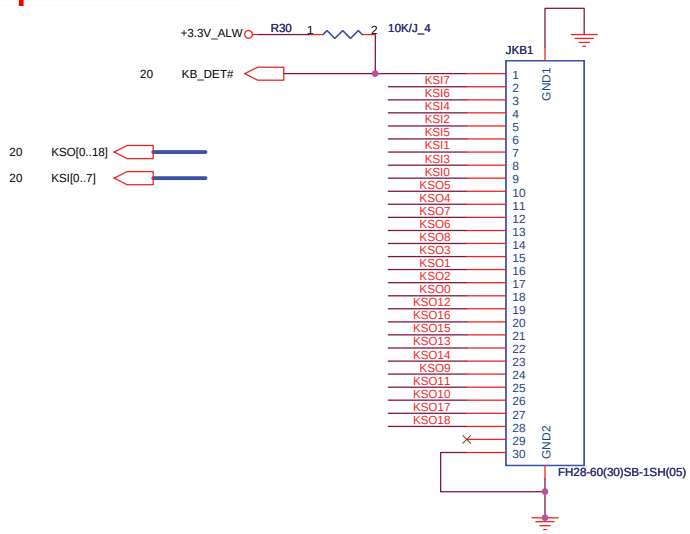


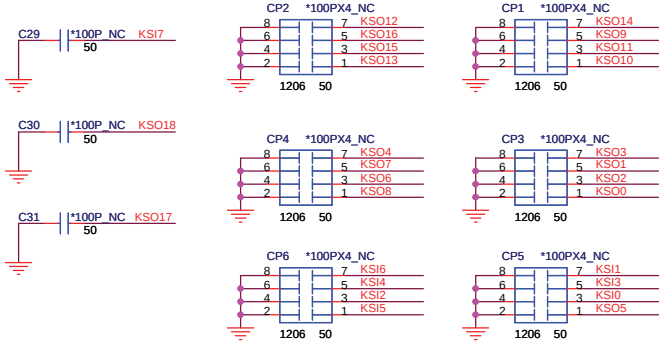
Key board illumination

+KB_LED power trace width >10 mil



KEYBOARD CONNECTOR





100P CAPS CLOSE TO JKB1

Quanta Computer Inc.
PROJECT : Calpella UMA

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	TP / KB	1A
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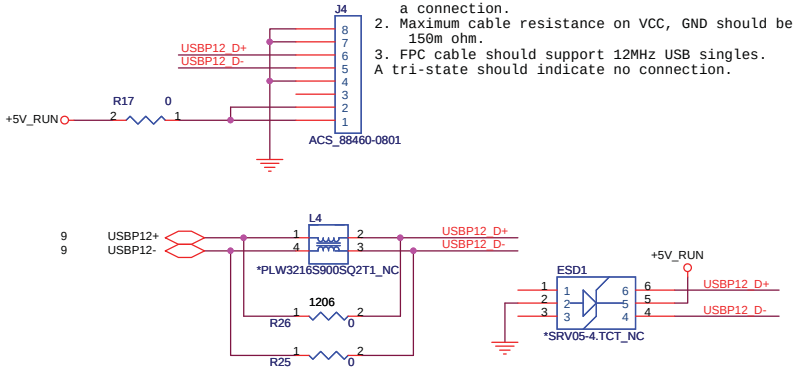
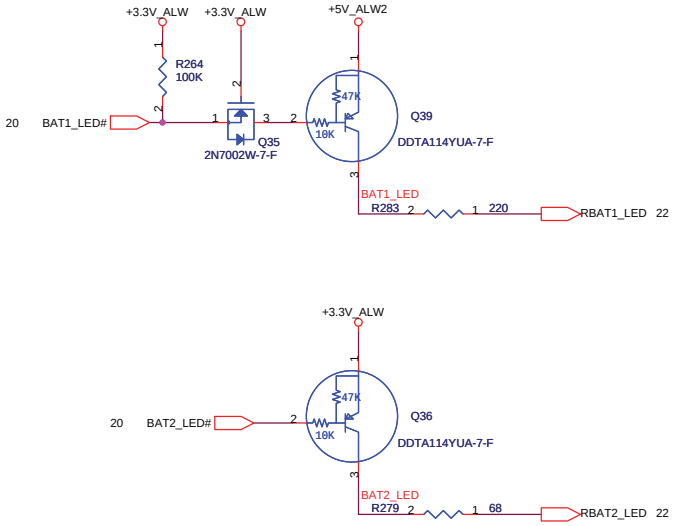
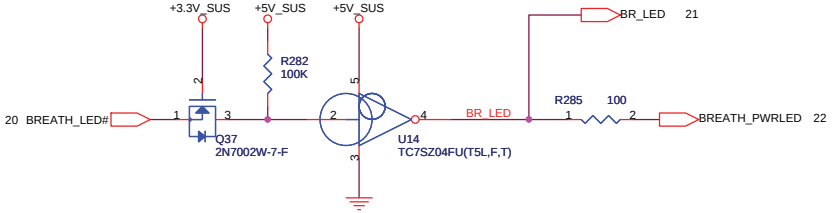
Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

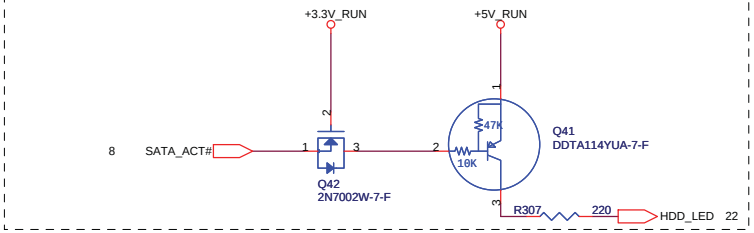


Battery status.

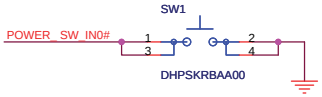




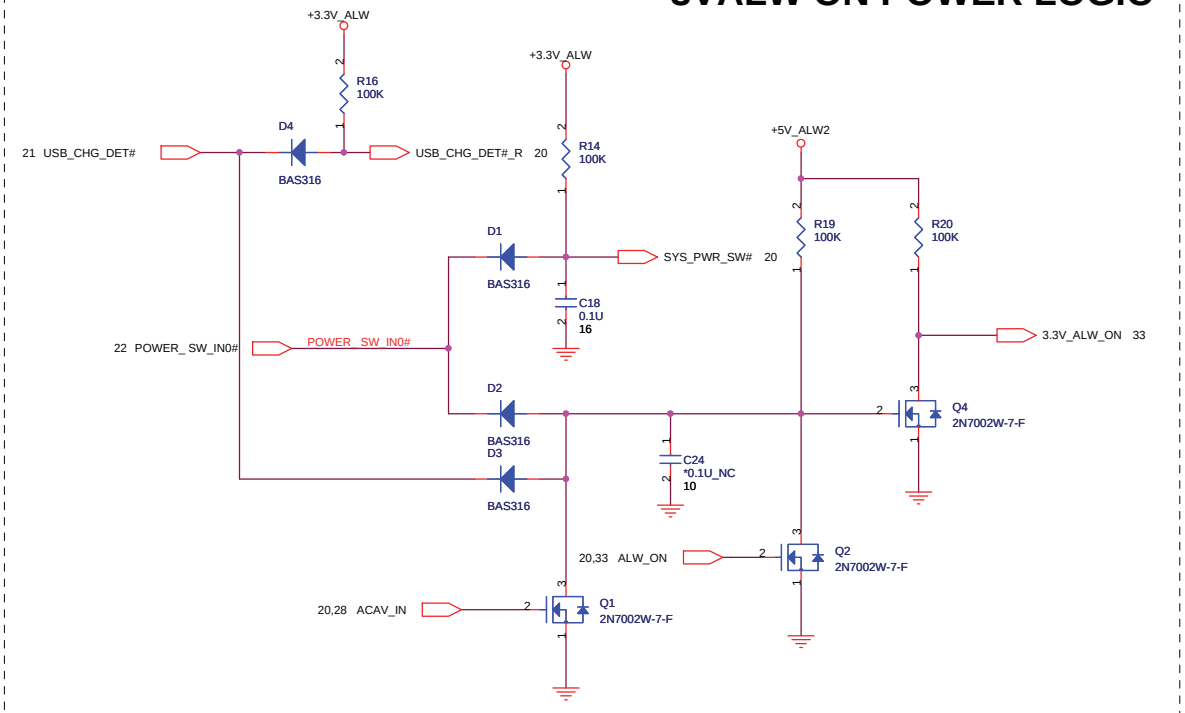
HDD activity LED.



Power button for Engineer



3VALW ON POWER LOGIC



Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	SWITCH / LED / T-Screen	1A
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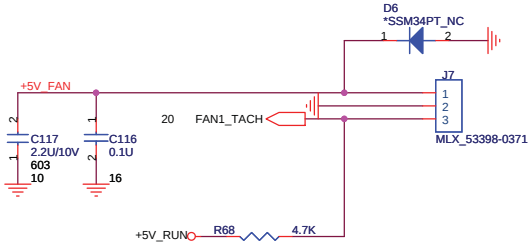
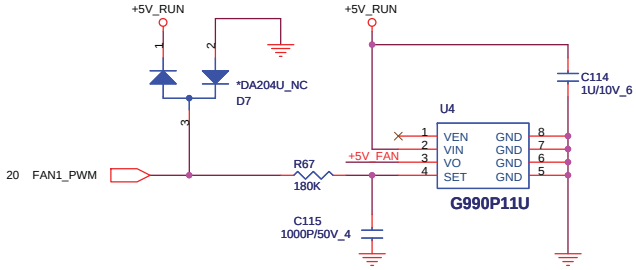
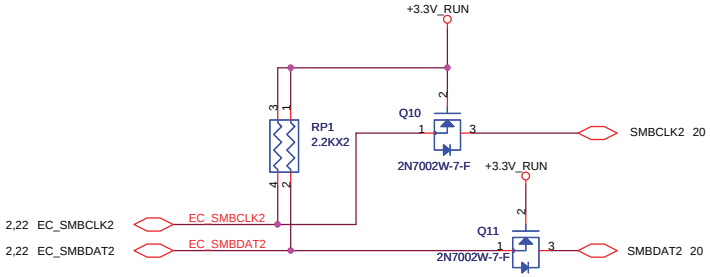
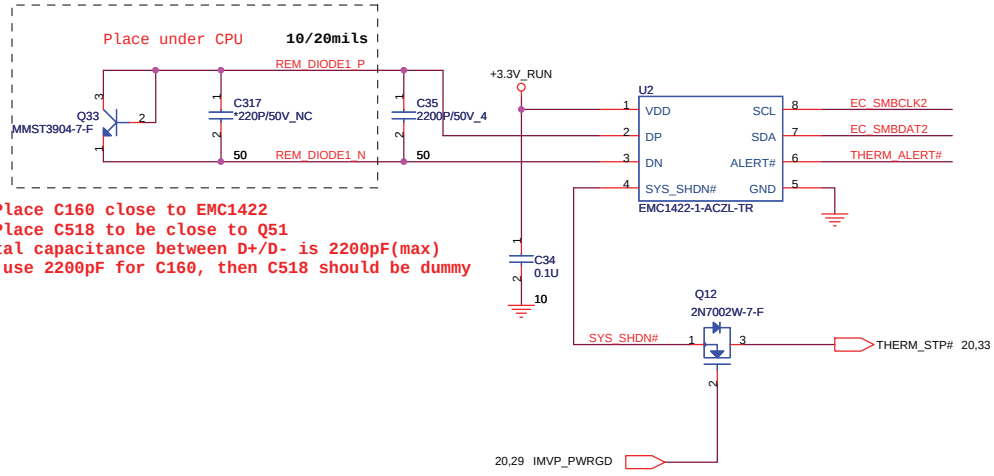


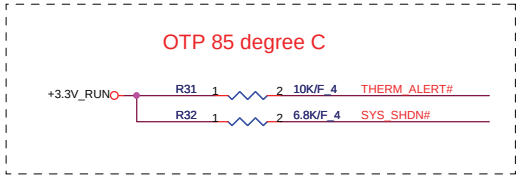




0907 Steg: Need to check C484 if needed



1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy



Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	FAN & THERMAL	1A
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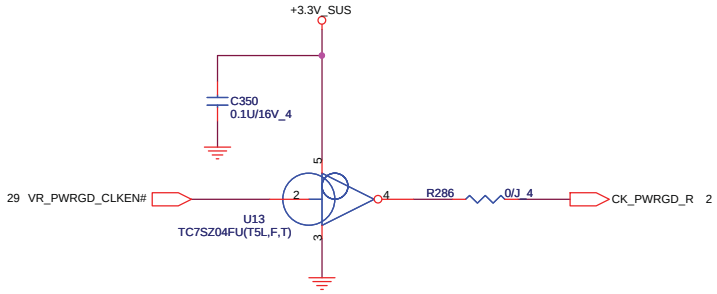

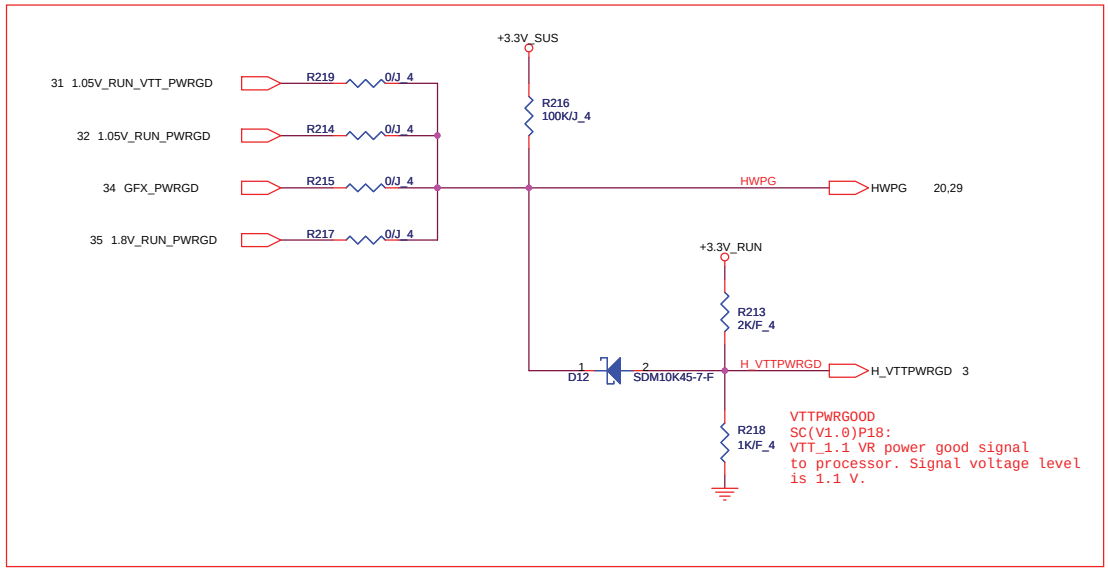

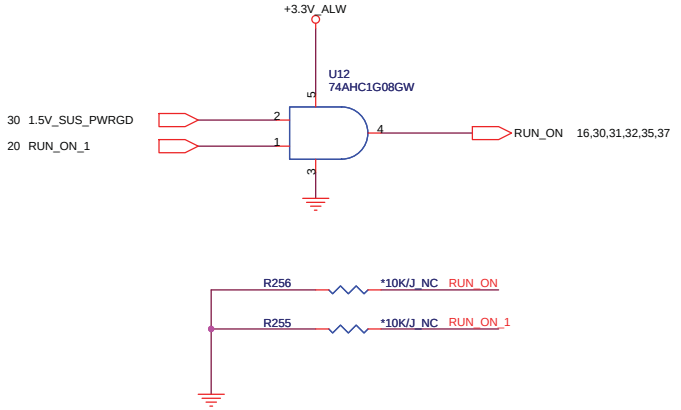

Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: System Reset Circuit	Rev: 1A
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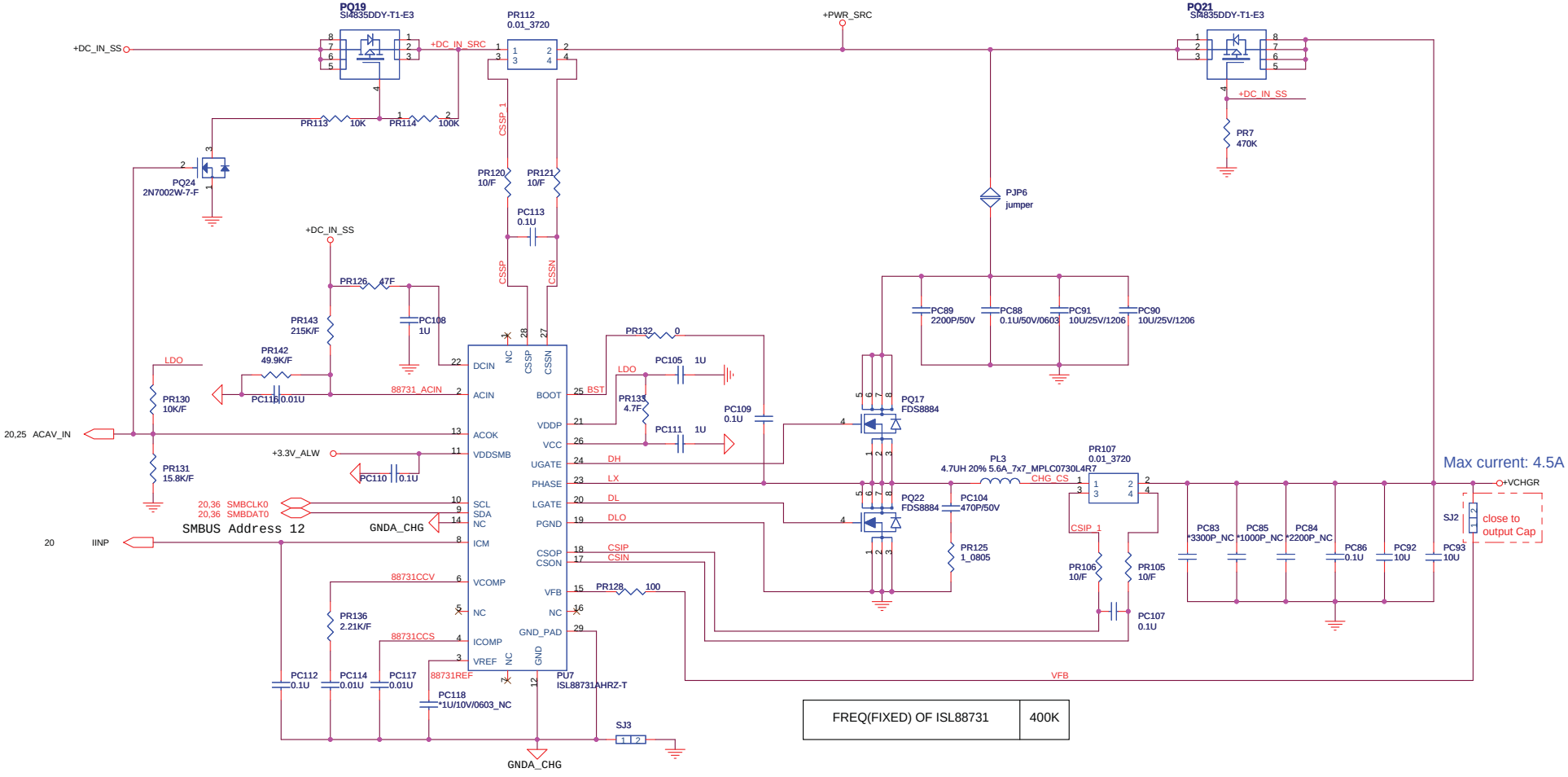

Quanta Computer Inc.
Project Name: XM2

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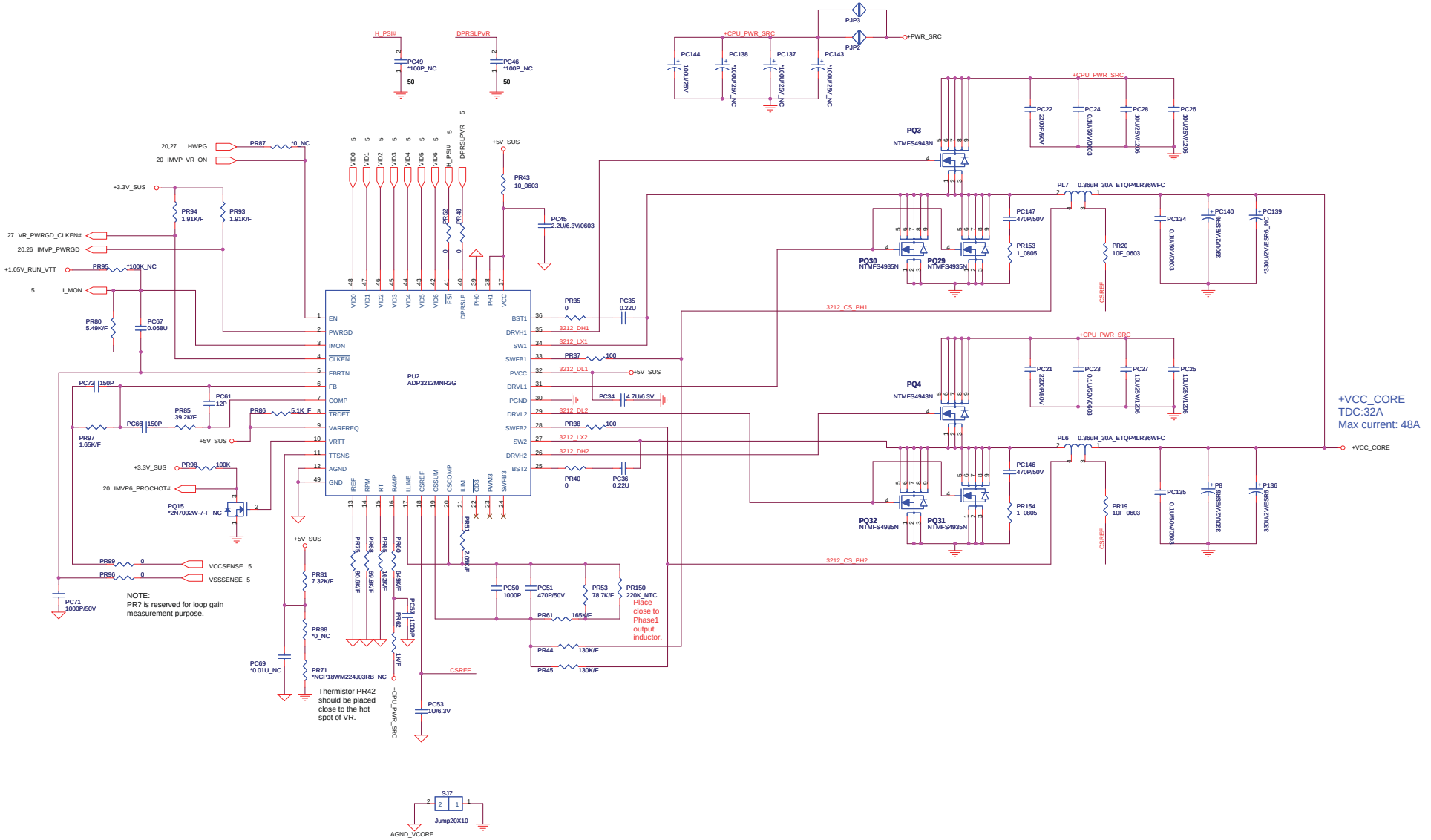

Quanta Computer Inc.			
Project Name: XM2			
Title: CoverPage			
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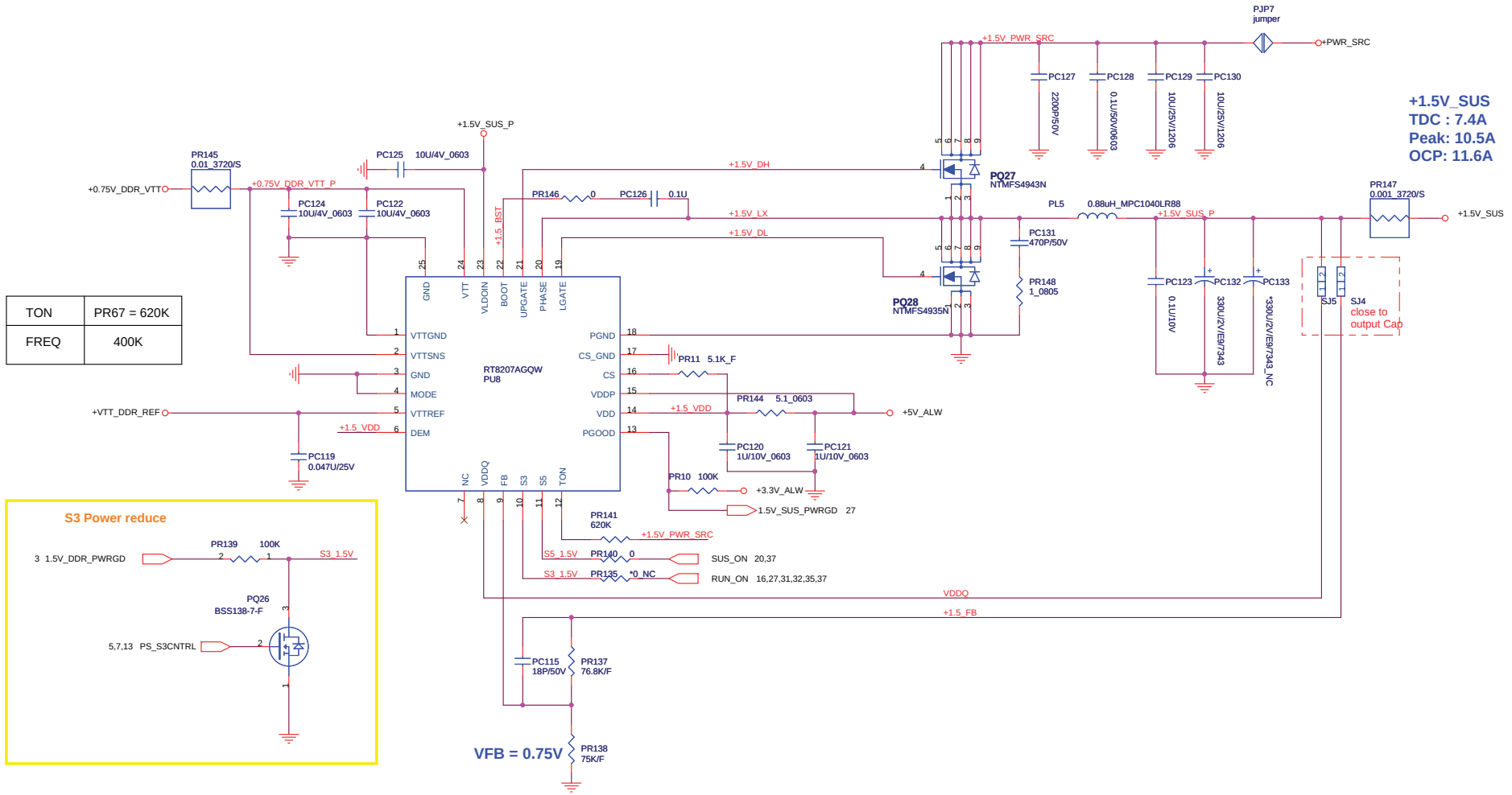

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection

FB	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
Project Name: XM2

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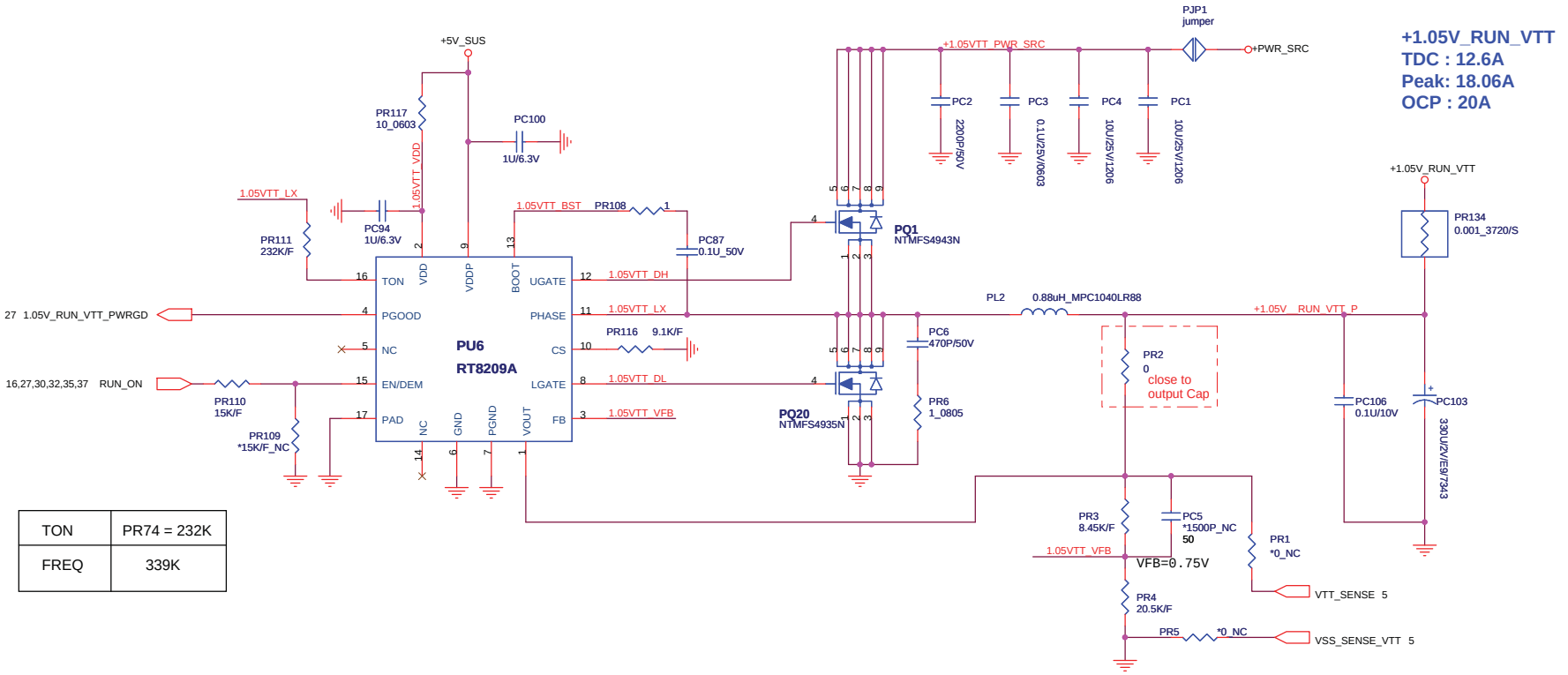

TON	PR74 = 232K
FREQ	339K

Quanta Computer Inc.

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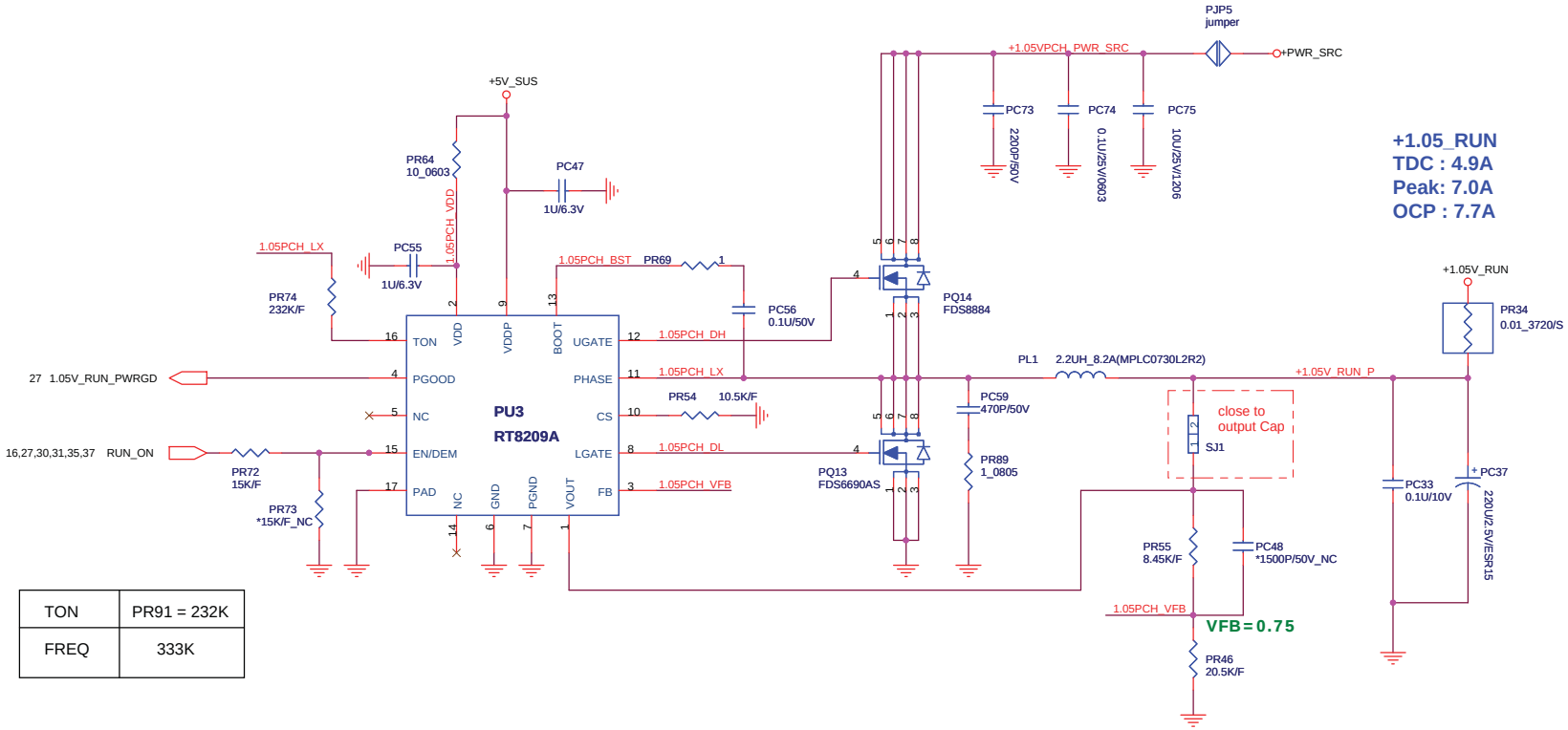

TON	PR91 = 232K
FREQ	333K

Quanta Computer Inc.

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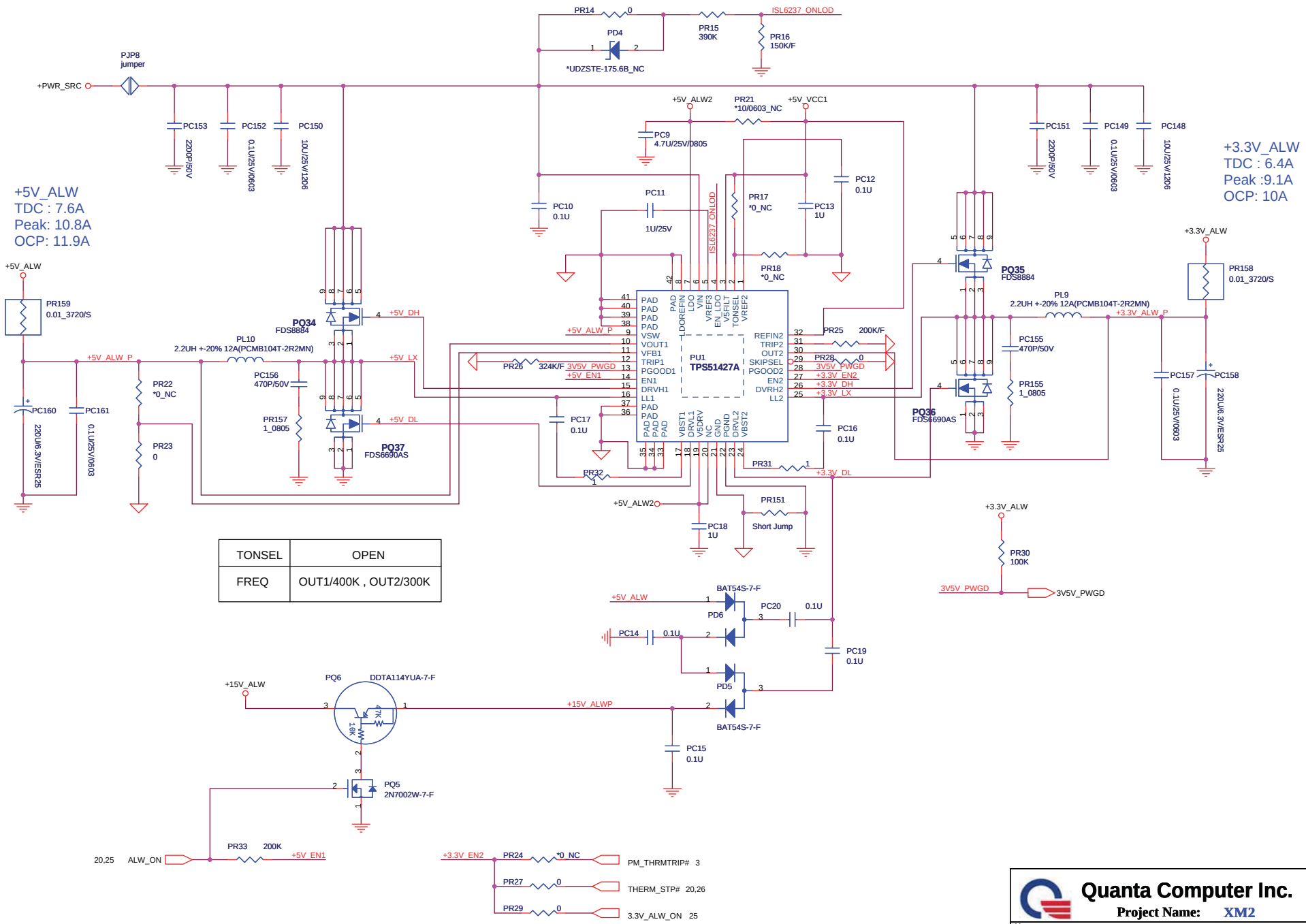

TONSEL	OPEN
FREQ	OUT1/400K , OUT2/300K

Quanta Computer Inc.	Project Name: XM2
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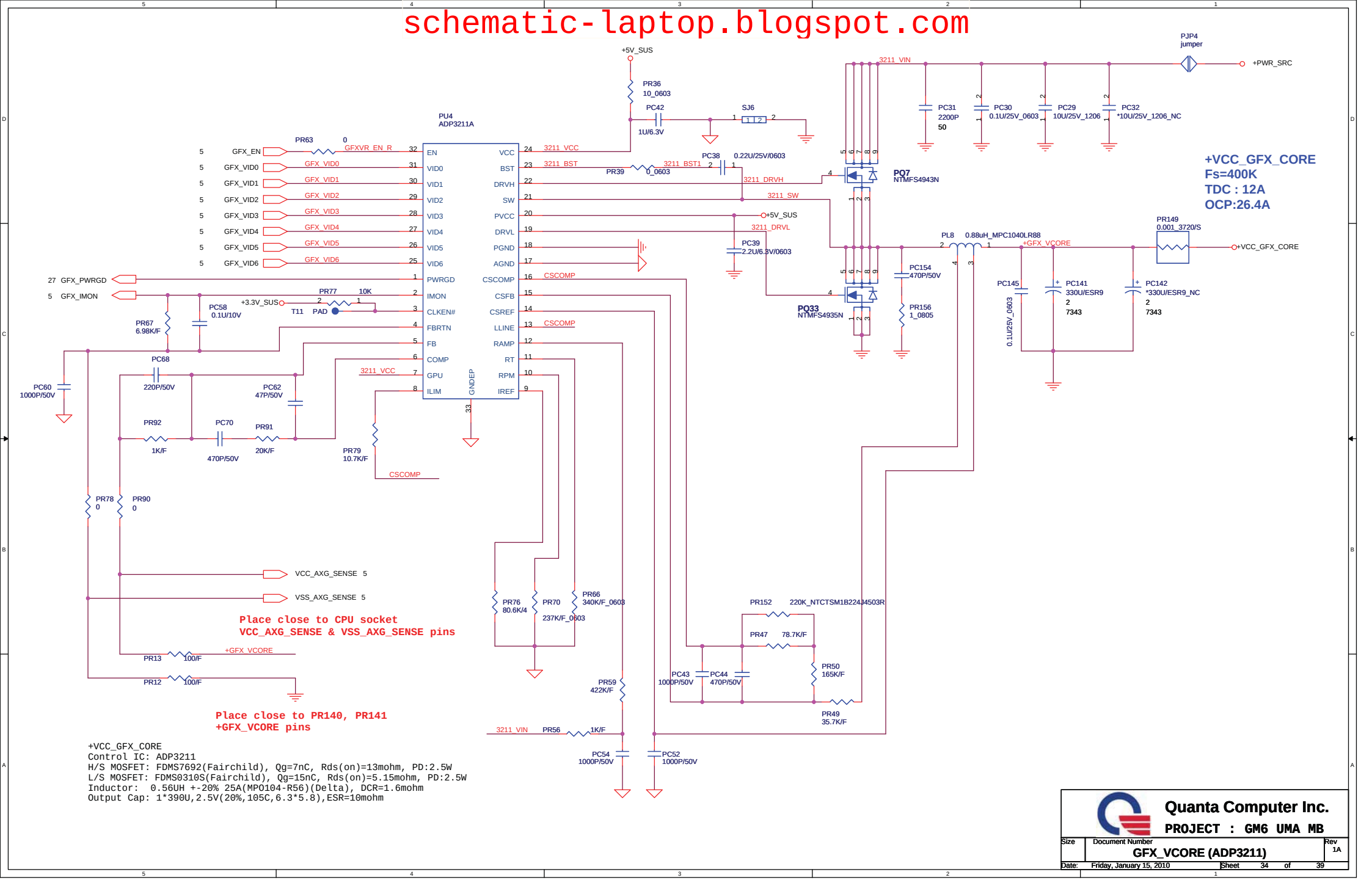

+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

Quanta Computer Inc.
PROJECT : GM6 UMA MB

Size	Document Number	Rev
	GFX_VCORE (ADP3211)	1A
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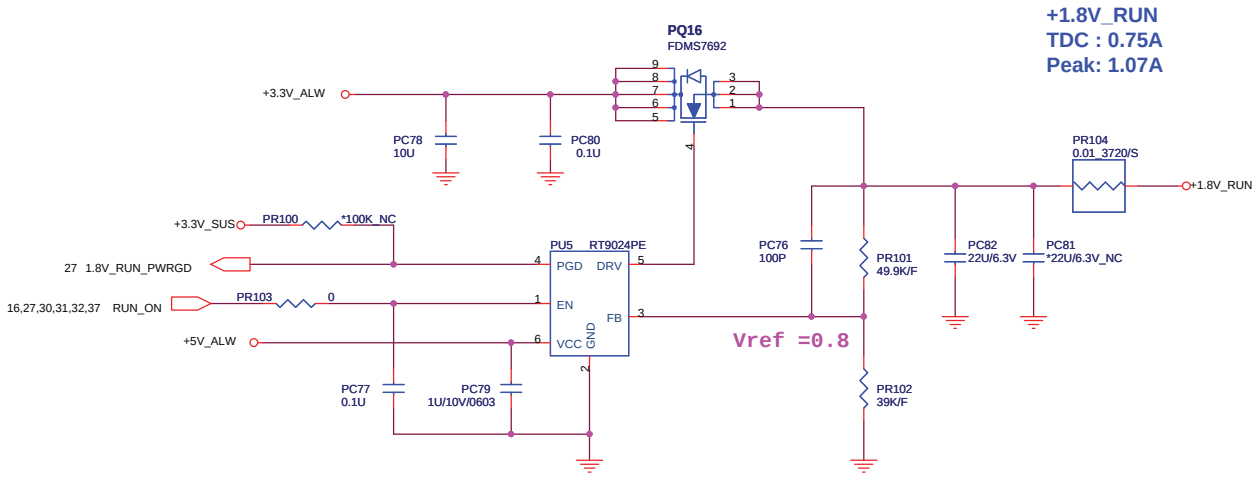

Quanta Computer Inc.		
Project Name: XM2		
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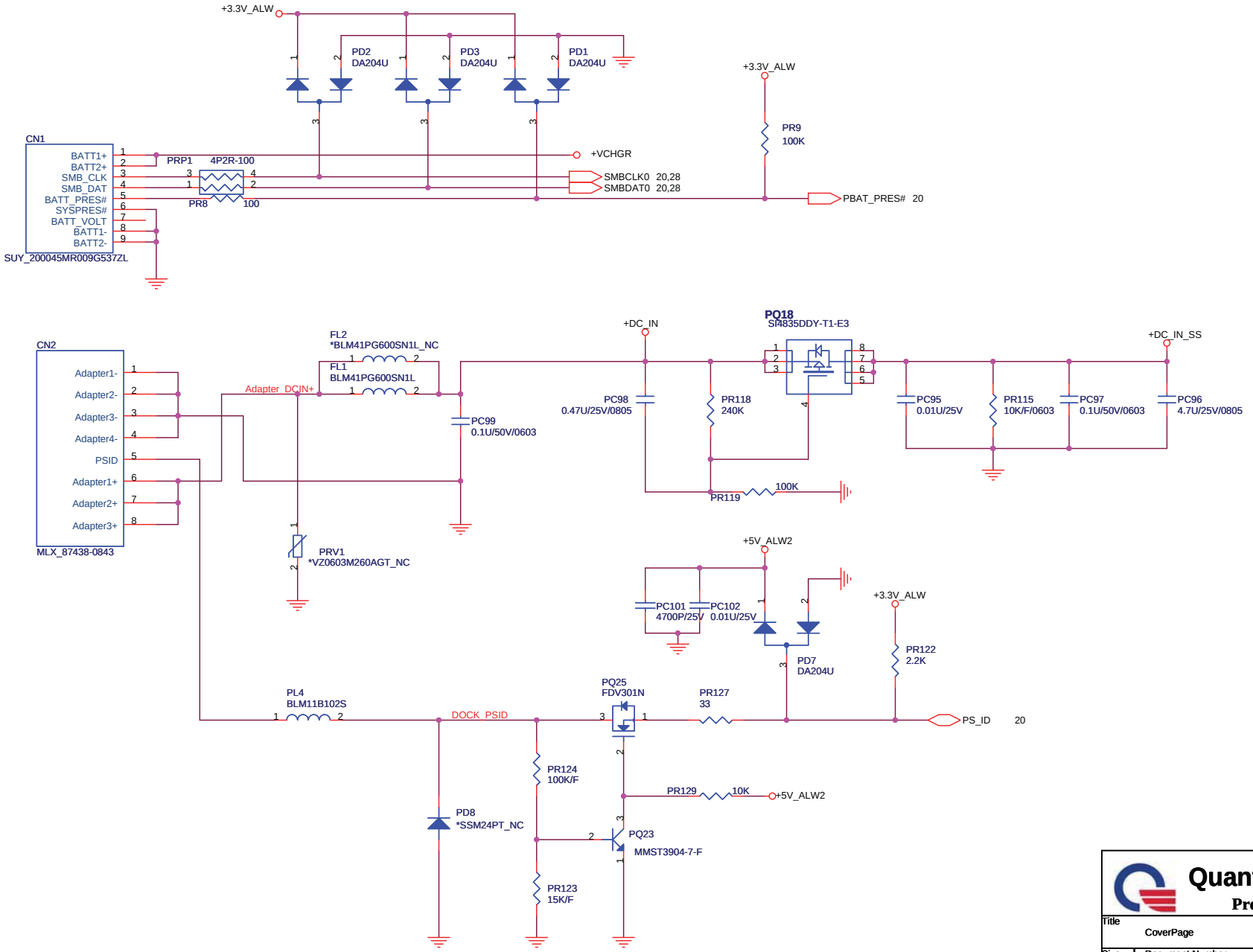

Quanta Computer Inc.

Project Name: XM2

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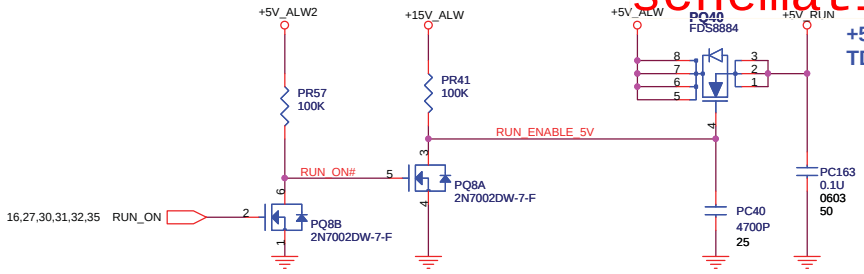
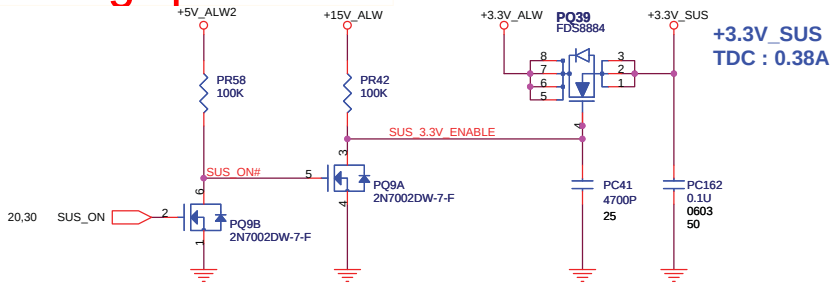
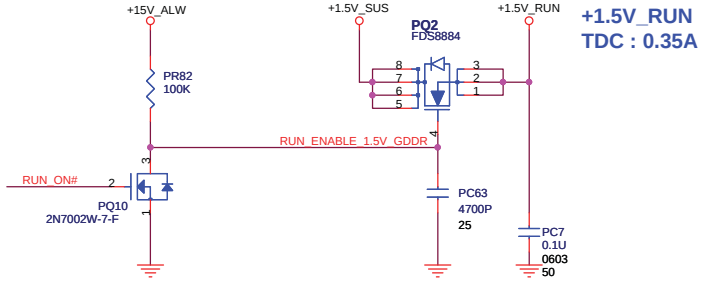
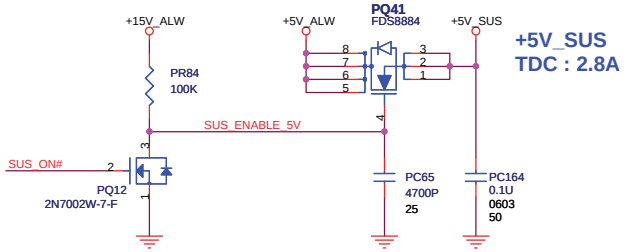
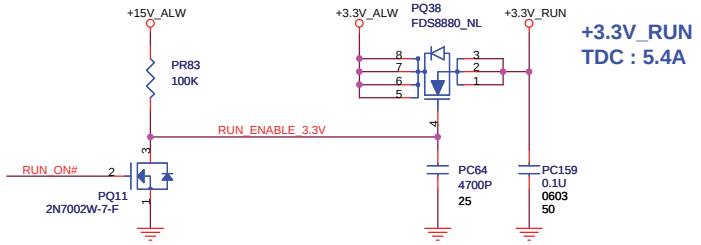


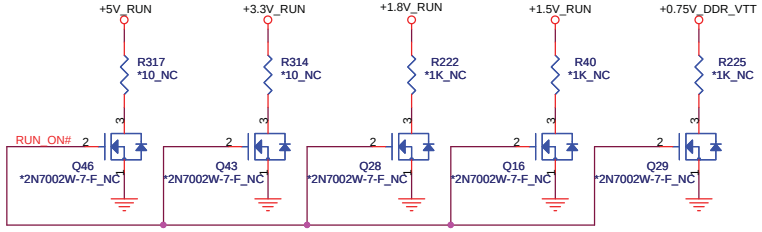


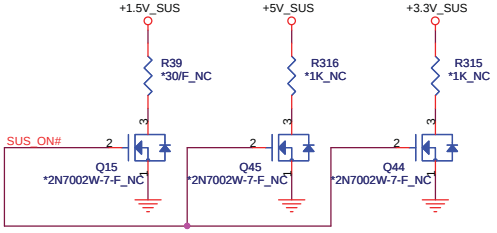






Reserve discharge path





Quanta Computer Inc.

Project Name: XM2

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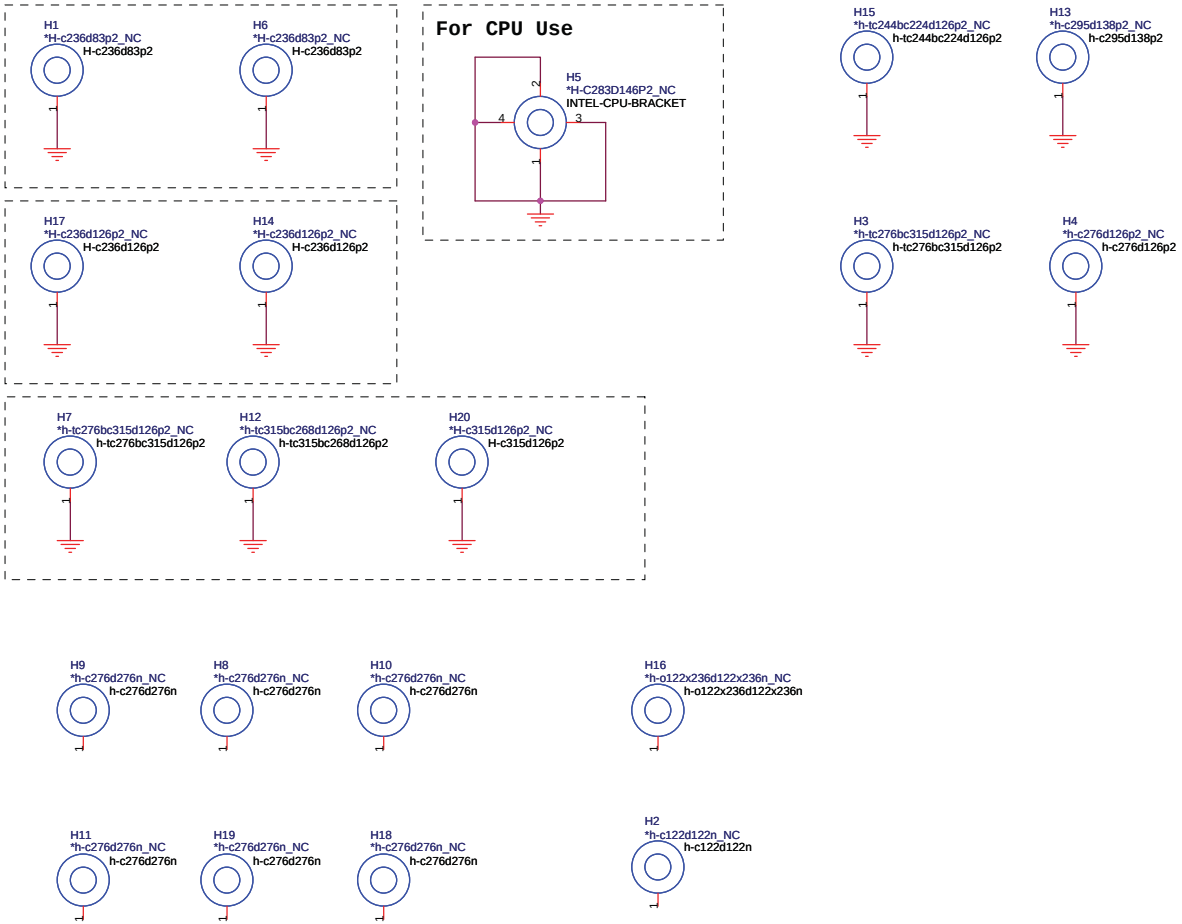

Quanta Computer Inc.

Project Name: GM7

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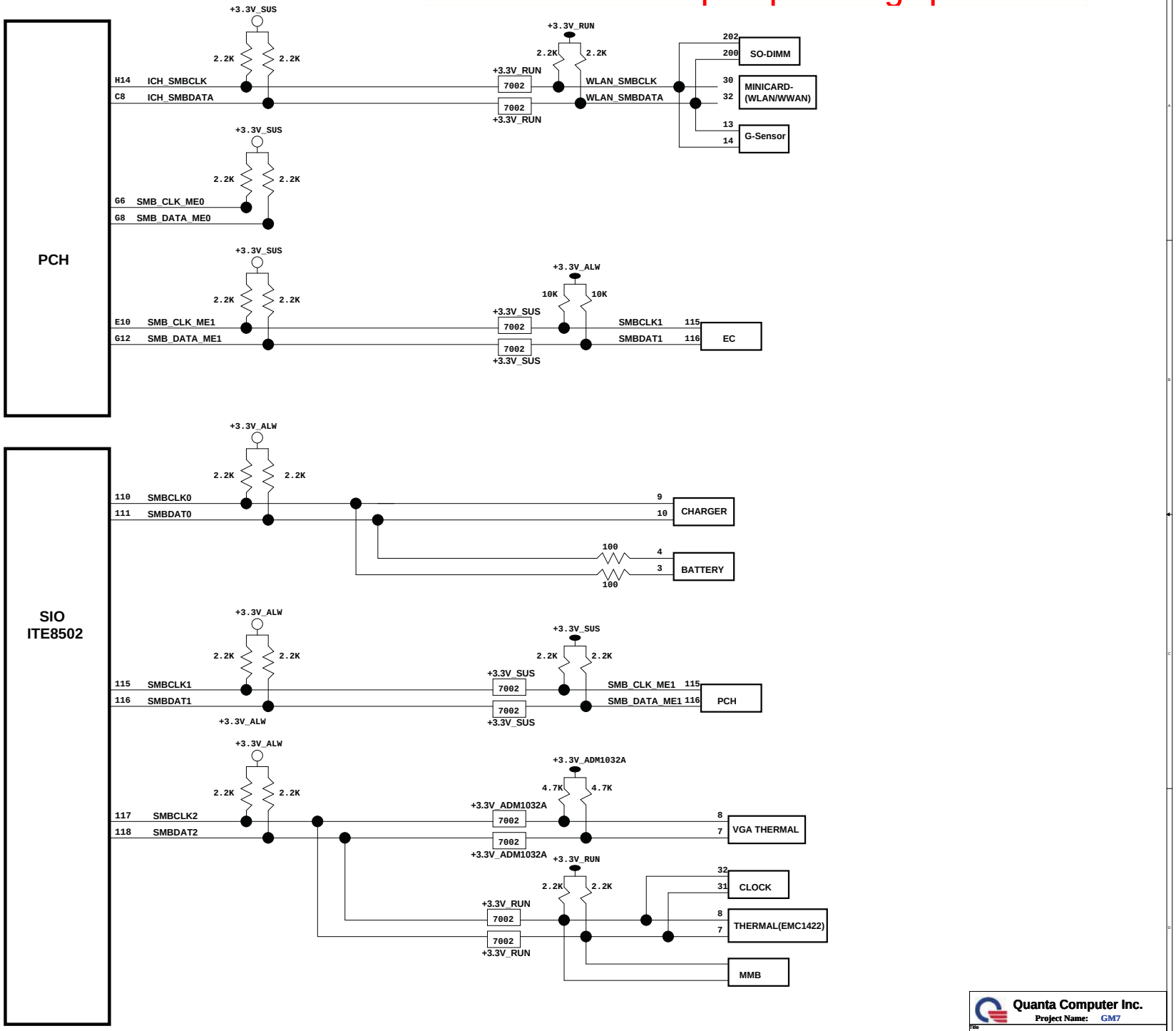

Quanta Computer Inc.
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Title: SMBus
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